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(54) **Interpolation device**

Interpolationsgerät

Appareil d'interpolation

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(73) Proprietor: **Sony Precision Technology Inc.**
Shinagawa-ku Tokyo (JP)

(72) Inventor: **Ishimoto, Shigeru,**
c/o Sony Magnescale Inc.
3-chome, Shinagawa-ku, Tokyo 141 (JP)

(74) Representative: **Grünecker, Kinkeldey,**
Stockmair & Schwanhäusser Anwaltssozietät
Maximilianstrasse 58
80538 München (DE)

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Description

[0001] The present invention relates to an interpolation device for a linear encoder or rotary encoder which is applied to an accurate length-measuring instrument and an accurate angle-measuring instrument.

[0002] In order to obtain highly divided interpolation such as above 100 division interpolation by means of an interpolation device for an encoder, various methods have been proposed and are in practical use. For example, there is an interpolation method using a phase modulation signal from a balanced modulator (disclosed in Japanese Patent Publication No. 5-18364), an interpolation method which executes interpolation by calculating arc-tangent of the input signals by means of a combination of an A/C converter and a digital computer, an interpolation method which obtains interpolation values by using an A/D converter and a look-up table (disclosed in a Japanese Patent Provisional Publication No. 49-106744), and an interpolation method which obtains interpolation values by using a special polar-coordinate transformation IC.

[0003] In the case that the interpolation is executed by using a phase modulation signal, it is necessary to provide a high-frequency interpolation clock and a high-speed logic circuit. Further, since the allowable limit of the response frequency must be smaller than ±5% of the carrier frequency to be balanced-modulated, this type of interpolation method is preferably not applied to an interpolation requiring a high-divisional interpolation and/or a high speed response.

[0004] Also, a conventional interpolation method using an A/D converter has a drawback such that when the A/D converter receives a signal from an encoder, the digital data outputted from the A/D converter frequently deviates at its lower several bits by each sample data due to the lack of a hysteresis characteristic. Therefore, this interpolation output signal varies (deviates) and is outputted as a high-order noise which puts the interpolation value unstable. In order to prevent such variation, the varying lower bits are rounded down and the rounded data is used, or two-times of necessary interpolation are executed and the obtained data is treated by a hysteresis lower than 1 resolution.

[0005] However, these methods require a resolution higher than a necessary resolution or higher processing ability in its processing section. Therefore, these methods increase the cost of the system.

[0006] EP-A-0 408 799 describes a position measuring system in which a sub-division circuit is used to interpolate data with greater precision. The sub-division circuit has a memory in which interpolation data is stored. Only part of the full range of possible values are stored and transformation tables are used to obtain an interpolated value.

[0007] Patent abstracts of Japan vol. 14, no 512 (E-0999), 8 November 1990 describes an A/D converter for converting an analog signal to a digital signal. After the output of the A/D converter has been processed by an eliminating device, the signal is filtered in a low pass type digial filter to eliminate high-frequency components.

[0008] It is an object of the present invention to provide an improved interpolation device which is free of the above drawbacks and performs a high resolution ability and high-speed interpolation using a relatively simple circuit.

[0009] An interpolation device according to the present invention is used for cyclic analog signals which periodically change their amplitude corresponding to a position function of a displacement. This object is solved by an interpolation device according to claim 1. Preferred embodiments of the invention are the subject matter of the dependent claims.

[0010] Fig. 1 is a block diagram of a first embodiment of an interpolation device according to the present invention.

[0011] Fig. 2 is a circuit diagram of a digital filter applied to the interpolation device of Fig. 1.

[0012] Fig. 3 is a block diagram of a modified example of the interpolation device of Fig. 1.

[0013] Fig. 4 is a circuit diagram of a hysteresis circuit applied to the interpolation device of Fig. 3.

[0014] Fig. 5 is a flowchart which shows a method for calculating an additive mean of inputted data.

[0015] Fig. 6 is a flowchart which shows a method for calculating a hysteresis.

[0016] Fig. 7 is a block diagram of a modified example of the first embodiment.

[0017] Fig. 8 is a block diagram of a modified example of the first embodiment.

[0018] Fig. 9 is a block diagram of a second embodiment of the interpolation device according to the present invention.

[0019] Fig. 10 is a table which shows a signal correction rule between phase A and phase B according to the fifth embodiment.

[0020] Fig. 11 is a table which shows a correction rule of a sine signal and a cosine signal.

[0021] Fig. 12 is a wave form graph for explaining an interpolation method for executing an interpolation by dividing one-cycle into odd multiples fo 4.

[0022] Fig. 13 is a wave form graph for explaining an interpolation method for executing an interpolation by dividing one-cycle into odd multiples of 8.

[0023] Fig. 14 is an explanatory view of a Lissajous figure which is formed when the amplitudes of the signals before interpolation are disposed on the x-y plane.

[0024] Fig. 15 is an explanatory view of interpolation data stored in a memory of the interpolation device of Fig. 9.

[0025] Fig. 16 is a table which shows the content of a look-up table for a phase A/phase B signal.

[0026] Fig. 17 is a table which shows a content of a look-up table for a 2-bits signal.

[0027] Figs. 18A to 18D are views for explaining the relationship among the quadrants.

[0028] Fig. 19 is a block diagram of a modified example of the second embodiment.

[0029] Fig. 20 is a circuit diagram which shows a quadrant conversion circuit of Fig. 19.

[0030] Fig. 21 is a circuit diagram which shows a correction circuit of the phase A and phase B data from the look-up table.

[0031] Fig. 22 is a circuit diagram which shows a difference value converter.

[0032] Fig. 23 is a circuit diagram which shows a UP/DOWN converter.

[0033] Fig. 24 is a circuit diagram which shows a A/B phase converter.

[0034] Fig. 25 is a circuit diagram which shows a circuit for outputting an absolute value upon accumulated adding of the difference values.

[0035] An interpolation device according to the present invention is arranged to eliminate a noise component in a high-frequency band of data from an A/D converter (analog-digital converter) by executing a filtering by means of a digital filter before the execution of an interpolation process. Further, this interpolation device comprises a hysteresis circuit with which a momentary deviation of the data is suppressed, in order to input stable data into an interpolation section. The A/D converter, which is normally applied to the interpolation device, outputs digital data whose lower several bits always deviate (vary) even if the input to the A/D converter is not changed. For example, if the A/D converter is 8 bit type and 2 Vp-p full scale, the resolution of the A/D converter becomes about 8 mV. In the case of a sound signal or visual signal, the influence of the noise is determined from a ratio between an amplitude of the signal and that of noise (S/N), and effective values of the signal and noise are compared. Therefore, it is not necessary to pay attention to the resolution in such a case. In the case of the signals of the encoder, such deviation at the lower several bits influences the signal as noise.

[0036] In the case that a comparator interpolates a signal from an encoder, a hysteresis of about 20 to 30 mV is applied to the signal in order to prevent the generation of drift of the output value. Accordingly, the A/D converter, which has a resolution of 8 mV, deviates within three or four values, that is, the A/D converter outputs the digital data which drifts at its two lower bits. Such drift of the digital data is suppressed by a digital filter and the filtered data is processed by an interpolation method, such as a calculation of an arc-tangent or an interpolation circuit using a look-up table.

[0037] Referring to Figs. 1 to 8, a first embodiment of the interpolation device according to the present invention is shown.

[0038] As shown in Fig. 1, an analog signal is inputted to an A/D converter 1 in order to be converted into a digital signal. The converted digital signal is inputted to a digital filter 2 wherein a high-frequency component of the converted digital signal is eliminated, that is, the several lower bits of the digital data are rounded (rounded up or rounded down). Then, the rounded digital data is inputted to an interpolation circuit 3 wherein an interpolation is executed.

[0039] The interpolation circuit 3 is basically constituted by a low pass filter. An additive mean may be obtained as a simple interpolation method, and it is well known that such a method is easily modified into a hardware.

[0040] Fig. 2 shows a typical digital filter where a plurality of delayed signals in synchronization with the signal of a clock are added in an adder 6. Such digital filter may be constituted by a computer. However, even if an analog filter is applied for processing a signal to be inputted to the A/D converter, the drift of data outputted from the A/D converter is not suppressed.

[0041] The manner of the operation for obtaining an additive mean with a computer will be discussed hereinafter with reference to the flowchart of Fig. 5.

[0042] At a step S1, the calculation for obtaining an additive mean is started.

[0043] At a step S2, a first address n of a memory is set to 1 (n=1).

[0044] At a step S3, new data is inputted to a position of a memory addressed by n.

[0045] At a step S4, data addressed by 1 to m are summed. A m-steps data adding filter is applied to this filter.

[0046] At a step S5, the sum of the data is outputted. With these steps S1 to S5, one filtering operation is completed and the routine proceeds to a step S10 wherein the routine comes to an end.

[0047] At a step S6, it is decided as to whether the filtering operation is repeated or not. When the decision at the step S6 is "YES", the routine proceeds to a step S7. On the other hand, wher the decision at the step S6 is "NO", the routine proceeds to a step S10 wherein the routine comes to an end.

[0048] In case that the operation is continued, the routine proceeds to the step S7 wherein the operation is delayed (waited) for a predetermined time period T.

[0049] At a step S8, n, which is indicative of a present address of the memory, is incremented by 1 (n=n+1).

[0050] At a step S9, it is decided whether n is greater than m or not. When the decision at the step S9 is "YES", the routine returns to step S2 to newly obtain the additive mean. When the decision at step S9 is "NO", the routine returns to step S3 in order to continue the operation for obtaining the additive mean.

[0051] With this calculation, the data to be interpolated is averaged, and stable digital signals are inputted to the interpolation section.

[0052] Almost all deviations of the digital data from the A/D converter 1 are constituted by white-noise components. Therefore, by executing sixteen-step additive mean operations by means of the digital filter, the noise component is

reduced to one-sixteenth of the white-noise. Accordingly, the deviation of the data, which has a deviation width of 4 bits, is decreased to a deviation width within 1 bit.

[0053] Generally, it is accepted that a group delay becomes long since a lot of samples are necessary for the execution at the digital filter. However, owing to the progress of digital video cameras for home-use, a high-speed A/D converter which processes video-band range data (up to about 20 Msps) has become comparatively inexpensive. Therefore, by using such an A/D converter, it becomes possible to execute the sixteen-step additive-mean process so that the group-delay is smaller than 1 μsec.

[0054] Although the elimination of noise contained in the output of the A/D converter can be executed by a digital filter, when the data inputted to the A/D converter takes a value which is close to a change point of a digital value, the lowest bit can change frequently. This change of the lowest bit can be suppressed by installing a hysteresis circuit. A hysteresis applied by such a hysteresis circuit is not an analog hysteresis obtained by a feedback to a comparator, but a digital hysteresis which is applied to the data executed at the A/D converter and the digital filter. This type of hysteresis circuit applied to the interpolation device according to the present invention is shown in Fig. 3.

[0055] The analog signal is converted into a digital signal at an A/D converter 1, and the converted digital signal is supplied to a digital filter 2 wherein the high-frequency component of the digital signal is eliminated. The signal processed at the digital filter 2 is supplied to a hysteresis circuit 4. The hysteresis circuit 4 applies a hysteresis characteristic to the digital signal so that the data is outputted as a stable digital signal. Such a digital signal is supplied to an interpolation circuit 3 wherein finely interpolated signals are obtained.

[0056] Fig. 4 shows a typical digital hysteresis circuit. The output of the digital filter is inputted to an input terminal 11. The signal is supplied to an input terminal A of a subtracter 17, an input terminal B of a comparator 14 and an input terminal A of a comparator 15. On the other hand, a hysteresis value is supplied to an input terminal 12. The signal is applied to an input end A of a selector 16 and an input end B of an adder 13. This hysteresis value is determined according to the degree of the rounding of the lower bits. Another input end B of the selector 16 receives "0". When the selector 16 receives a high-signal at a control terminal S from the comparator 15, the input signal A is outputted from the selector 16 to another input B of the subtracter 17. When the selector 16 receives a low-signal at the control terminal S, the zero signal is outputted.

[0057] The subtracter 17 obtains a difference between the output of the digital filter 2 and the output of the selector 16. The difference obtained at the subtracter 17 is supplied to a register circuit (flip-flop circuit) 19. The output of the register circuit 19 is treated as an output of the digital hysteresis circuit 4 and is inputted (feedbacked) to an input end A of the comparator 14 and to an input end A of the adder 13. The comparator 14 executes a comparison between the value stored in the register circuit 19 and the inputted digital signal. When the value stored in the register is larger than the input digital value (A>B), the comparator 14 outputs 1 as an output logical value to an enable signal port of the register circuit 19 through an OR circuit 18 so that the register circuit 19 stores the output of the subtracter 17. This storage of the output of the subtracter 17 is executed in synchronization with the system clock.

[0058] When the signal from the register circuit 19 is smaller than the input digital signal, the comparator 14 outputs 0 as a logical value. That is, since the register circuit 19 does not receive an enable signal, the content of the register circuit 19 is not changed.

[0059] On the other hand, the output of the register circuit 19 is applied to the input end A of the adder 13. The adder 13 adds the register stored value and the hysteresis value. The result of the adder 13 is applied to an input end B of the comparator 15. The comparator 15 compares the inputted digital data and the output of the adder 13. When the inputted digital data is larger than the output of the adder 13, the comparator 15 outputs a logic signal 1 as a high-level signal to selector 16 so that the selector 16 outputs a hysteresis value to the subtracter 17.

[0060] The subtracter 17 supplies the difference between the inputted digital data and the hysteresis value to the register circuit 19. In this condition, the output logical value of the comparator 15 is set at 1, and the enable signal is applied to the register circuit 19 through the OR circuit 18. Therefore, the digital signal, which is the output of the subtracter 17, is stored in the register circuit 19.

[0061] When the input digital signal is smaller than the sum of the register stored value and the hysteresis value, the comparator 15 outputs 0 as an output logical value. Therefore, the register circuit 19 keeps the previous value.

[0062] Fig. 6 shows an operation of the digital hysteresis circuit 4 of Fig. 4.

[0063] At a step S11, the operation of the digital hysteresis circuit 4 is started.

[0064] At a step S12, it is decided whether or not the present input data is smaller than the previous input data. When the decision at step 12 is "YES", the routine proceeds to a step S15 wherein the present data is stored as new data. Then, the routine proceeds to a step S16 wherein the routine ends.

[0065] When the decision at step S12 is "NO", the routine proceeds to a step S13 wherein it is decided whether or not the present data is larger than the sum of the previous data and the hysteresis value. When the decision at the step S13 is "YES", the routine proceeds to a step S14 wherein the present data is decremented by the hysteresis value (present data = present data - hysteresis value). Following this, the routine proceeds to step S15 wherein the present data is stored as new data. When the decision at the step S13 is "NO", the routine proceeds to step S16 wherein the

routine comes to an end.

[0066] This digital hysteresis circuit is arranged so that the present data is compared with the data stored in the register circuit by using a comparator, an adder, a subtracter and a register circuit (flip-flop circuit). When the present data is smaller than the register stored data, the present data is stored in the register circuit as it is. When the present data is larger than the sum of the register storing data and the hysteresis value, the result of a subtraction of the hysteresis value from the present data is stored in the register circuit. The operation of this hysteresis circuit may be constructed a program executed by a computer.

[0067] Fig. 7 shows a modified example of the first embodiment of the interpolation device for multi-phase signals in accordance with the present invention. As shown in Fig. 7, the multi-phase signals are A/D converted by a plurality of A/D converters 1 for each phase signal (IN1, IN2, — , INn). The A/D converted signal are processed by the respective digital filters 2 and the respective hysteresis circuits 4, as mentioned above. Then, the processed signals are inputted to the interpolation circuit 3.

[0068] Fig. 8 shows another modified example of the first embodiment of the interpolation device for processing multi-phase signals in accordance with the present invention. In this example, an A/D converter, a digital filter and a hysteresis circuit are used sharingly for each phase signal of the multi-phase signals. As shown in Fig. 8, each signal is inputted and kept at each sample-and-hold circuit (SH1, SH2, — SHn) 35. A timing-signal generator (TG) 37 controls the connection between each sample-and-hold circuit 35 and the A/D converter 31 by a switch 36. The contents in the sample-and-hold circuits 35 are, in turn, supplied to the A/D converter 31. Then, the A/D converted data are in turn supplied to the digital filter 32 for eliminating a high-frequency component of each data. The filtered data is supplied to corresponding registers (R1 to Rn) 38. The stored data is supplied to the interpolation circuit 33 in parallel.

[0069] Referring to Figs. 9 to 25, a second embodiment of an interpolation device according to the present invention is shown.

[0070] As shown in Fig. 9, a pair of input signals are inputted from input terminals 101 and 102 to A/D converters 103 and 104 respectively. The digitized data is supplied to digital filters 105 and 106 wherein high-frequency components of the respective converted digital signal are eliminated, that is, several lower bits of the digital data are rounded (rounded up or rounded down). Then, the rounded digital data is inputted to a quadrant conversion section 107 where the quadrant on the x-y coordinate of each digitized data is searched in order to decrease a data volume of a look-up table 108. That is, by taking into account the changing direction of the data in each quadrant, the look-up table 108 for one quadrant is applied to other data in other quadrants. In a correction section 109, such correction of the data obtained at the look-up table 108 is corrected according to the quadrant position of the inputted signals from the quadrant conversion section 107.

[0071] Analog signals outputted from an encoder are periodic signals which are shifted in phase by 90° and form a relationship of a sine wave and a cosine wave. The amplitude of each analog signal is digitized by an A/D converter. The digitized data is inputted to a ROM in the form of the look-up table 108 of the data and the address of lower address and upper address. Therefore, by using this look-up table, the interpolation of the data is executed.

[0072] As shown in Fig. 14, assuming that the horizontal axis is x-axis, the vertical axis is y-axis, a circle around the origin point of the x-y coordinate is formed to have a radius r, and the rotation angle is ω. The above mentioned sine and cosine waves have the following relationship with the x-y coordinates.

$$y = r \sin \omega t$$

$$x = r \cos \omega t$$

[0073] In Fig. 14, numerals I, II, III and IV represent first to fourth quadrants, respectively. The quadrants I and IV as are axially symmetric with respect to the x-axis. The quadrants II and III are axially symmetric with respect to the x-axis. Therefore, the pair of data units of the corresponding quadrants take the same values at the x value. Similarly, the quadrants I and II are axially symmetric with respect to the y-axis. The quadrants III and IV are axially symmetric with respect to the y-axis. Therefore, the pair of data units of the corresponding quadrants take same values at the y value.

[0074] As shown in Fig. 14, x values of the quadrant II and the quadrant III are defined to be within 000 to 1FF, the x values of quadrant I and quadrant IV are defined to be within 200 to 3FF, y values of quadrant IV and quadrant III are defined within 000 to 1FF, and the y values of the quadrant I and the quadrant II are defined to be within 200 to 3FF.

[0075] Comparing the x, y values in the quadrant I with the x, y values in the quadrant II, y values of the quadrant I and the quadrant II take 200 to 3FF, and x values of the quadrant I take 200 to 3FF and x values of the quadrant II take 000 to 1FF. Therefore, except for the most significant bit, the other bits take the same values in both the quadrant I and the quadrant II. This indicates that it is possible to permute the data of the quadrant II by the data of the quadrant I.

[0076] Further, in the quadrant III, x values range from 000 to 1FF and y values range from 000 to 1FF. In the quadrant IV, x values range from 200 to 3FF and y values range from 000 to 1FF. Accordingly, it is possible to permute such data of the quadrant III and the quadrant IV by the data in the quadrant I.

[0077] Fig. 15 shows a digital data unit of a representative quadrant. The quadrant (quarter circle) shown in Fig. 15 is formed so that the address values are arranged to increase from left to right and from lower to upper in the drawing. This can be directly applied to the data in the quadrant I. As to the data in the quadrant II, this data stored in the ROM is not directly applied. It is necessary to execute a conversion of the data as shown in Figs. 18A to 18D.

[0078] Fig. 18A shows base data stored in the ROM. Since it is assumed that the base data stored in the ROM is of the quadrant I, $1/2\pi$ rotated data of the quadrant II are equivalent with those of the quadrant I. Therefore, the data of the quadrant II may be represented as shown in Fig. 18B. Herein, since the vertical axis is arranged so that the number is increased from upper to lower, it is necessary to invert these data. Although in Fig. 18A the horizontal axis corresponds to cosine and the vertical axis corresponds to sine, in Fig. 18B the horizontal axis corresponds to sine and the vertical axis corresponds to cosine. Therefore, it is necessary to replace these axes. Since 180° rotated quadrant III is equivalent with the quadrant I, the quadrant III is represented as shown in Fig. 18C. However, the increasing directions of both of the x-axis and the y-axis are the inverse of those of the quadrant I.

[0079] 270° rotated quadrant IV is equivalent with quadrant I except that the increasing direction of the horizontal axis of Fig. 18D is inverse to that of Fig. 18A. Accordingly, it is necessary to invert this direction. In addition, although Fig. 18A shows that the horizontal axis is cosine and the vertical axis is sine, Fig. 18D shows that the horizontal axis is sine and the vertical axis is cosine. Further, it is necessary to distinguish four quadrants from the uppermost bit of the address bits.

[0080] Fig. 11 shows remarking points for the conversion. In the table 1 of Fig. 11, sc denotes the most significant bit of the sine signal and the cosine signal which are represented by 11, 10, 00 and 01 corresponding to the quadrants I to IV. In the address blocks, lined sin and cos, namely, $\overline{\sin}$ and $\overline{\cos}$ represent complement values (inverted number).

[0081] As a method for substituting the interpolation data of sine and cosine waves for one-cycle (360°) by the data of 1/4 cycle (90°), for example, considering the Lissajous figure formed on the x-y plane by the data of sine and cosine waves whose data length is 10 bits, in order to represent the four quadrants by the quadrant I on the Lissajous figure, the data except for the most significant bit is changed according to the most significant bit of the data of the sine and cosine waves so that the address changing direction of the other quadrants corresponds to that of quadrant I. More particularly, when the most significant bit is 0, the data except for the most significant bit is inverted. Further, when the data of the sine and cosine waves of the even numbered quadrants are exchanged with each other.

[0082] Since the data length is 10 bits, that is, 10 character binary number which can be represented as 000 to 3FF with hexadecimal numbers, the replacement is executed according to the condition of the most significant bit while the lower 9 bits are inverted. Further, Fig. 11 shows a truth table of this embodiment. The relationship among the interpolation data of a look-up table stored in the ROM, the lower address and the upper address are represented by the following equations.

$$\text{Interpolation data} = \arctan(\text{lower address}/\text{upper address})$$

$$\text{interpolation number} / 2\pi, \text{ wherein lower address} \geqq \text{upper address.}$$

$$\text{Interpolation data} = \text{interpolation number}/4 - \arctan$$

$$(\text{upper address}/\text{lower address}) \cdot \text{interpolation number}/2,$$

$$\text{wherein lower address} < \text{upper address.}$$

[0083] Further, wherein the x-axis denotes the upper address and the y-axis denotes the lower address, it will be understood that the relationship between the axis and the address may inverted.

[0084] Fig. 19 shows a modified example of the second embodiment of the interpolation device. In this circuit, the sine signal and cosine signal are inputted to A/D converters 201 and 202 from a sensor (not shown). The A/D converters 201 and 202 convert the received analog signals into digital signal according to a sampling signal from a clock 203, and output to digital filters 221 and 222 wherein high-frequency components of the respective converted digital signal are eliminated, that is, the several lower bits of the digital data are rounded (rounded up or rounded down). Then, the rounded digital data is inputted to a quadrant conversion section 204.

[0085] The quadrant conversion section 204 generates a distinguish signal for distinguishing the quadrant of the input signal from the uppermost bit of the input signal, and sends the distinguish signal to an offset selector 207. Further,

the quadran converter 204 generates an address signal corresponding to the data in the quadrant I from the absolute value of the sin and cos signals, and supplies it to a look-up table 205 as an address signal of the look-up table 205.

[0086] The look-up table 205 has stored interpolation data and outputs a selected data according to the commanded address. Corresponding to the above-mentioned quadrant, first to fourth memory units 208 to 211 respectively store an offset value of the quadrant I, an offset value of the quadrant II, an offset value of the quadrant III, and an offset value of the quadrant IV. The first to fourth memory units 208 to 211 are connected to the offset selector 207 so that one of the memory unit is selected according to the command of the selector 207.

[0087] The offset values of the first to fourth quadrants are selected such that the quadrant I is 0, the quadrant II is 1/4, the quadrant III is 2/4, and the quadrant IV is 3/4. The selected offset value is added to the data selected at the look-up table 205 in an adder 206. The calculated data is outputted as position data.

[0088] Fig. 20 shows a circuit diagram of the quadrant conversion section 204 of Fig. 19. Binary signals outputted from the A/D converter corresponding to the amplitude of the sine wave and the cosine wave supplied from the displacement detector are inputted to the quadrant conversion section 204. Although in this figure one input terminal is denoted by each sine and cosine, practically nine terminals are provided for each sine and cosine signal. The inverter outputs a logical value 0 when the corresponding bit indicates 1. When the corresponding bit indicates 0, the inverter outputs a logical value 1. AND is a conjunction circuit, OR is a disjunction circuit. This circuit outputs a truth value as shown in Fig. 11.

[0089] Fig. 22 shows a circuit diagram which outputs a difference value which is obtained by storing data for one cycle of the output of the interpolation circuit and the output of the adder and by subtracting each of them from the previous sampled data.

[0090] This circuit for obtaining a difference value is set to the output side of the interpolation circuit of Fig. 19. In this circuit, the input position data is supplied to an input terminal 321 and supplied to a flip-flop circuit (F/F) 323 according to a sampling clock inputted from a terminal 322. Accordingly, the output of the flip-flop circuit 323 represents data obtained in a previous sampling time.

[0091] A difference between the present data and the previous data is obtained at a subtracter 324. The difference value indicative of a difference of an anticlockwise moving direction on the Lissajous figure is outputted. Similarly, a difference between the present data and the previous data is obtained at a subtractor 325. The difference value indicative of a difference of a clockwise moving direction on the Lissajous figure is outputted. The output of the subtracter 324 is inputted to an input end of a comparator 326 wherein the input difference signal is compared with a maximum difference signal inputted from another input end of the comparator 326. When it is decided that the input difference signal is larger than the maximum difference, the comparator 326 outputs a high-level signal so as to turn on one input end of an AND circuit 334. The AND circuit 334 outputs an error signal when a high-level signal is inputted to one of its input ends.

[0092] Similarly, the output of the subtracter 325 is inputted to an input end of a comparator 332 wherein the input difference signal is compared with a maximum difference. When it is decided that the input difference signal is larger than the maximum difference, the comparator 332 outputs a high-level signal to the AND circuit 334.

[0093] If the difference signal is not larger than the maximum difference, the output level of the comparators 326 and 332 are set to a low level. Therefore, the output of AND circuits 328 and 329 are turned on, and the difference value is outputted from an OR circuit 330. At this time, the output of the comparator 332 is a difference of a clockwise direction. Therefore, by outputting the difference, the indication of the direction is executed.

[0094] It will be understood that an absolute value of an encoder is obtained by the accumulated sum of the output of the difference value conversion circuit. Fig. 25 shows an example of an accumulated adder applicable to this case. As shown in Fig. 25, according to the direction signal inputted to an input terminal 351, the difference signal from the difference conversion circuit is inputted from the difference converter to an adder 353 so as to be added to the previous value. Therefore, the absolute value of the encoder is outputted to an output end 355.

[0095] Fig. 23 shows an UP/DOWN conversion circuit for obtaining A/B phase by inputting the difference value to a programmable timer. The difference value inputted to an input terminal T2 is supplied to a programmable gate timer C1 which in the difference signal is converted into a on and off signal according to a clock signal from a standard oscillator. The output of the programmable gate timer is applied to AND circuits A1 and A2. The direction signal is applied from an input terminal T3 to the AND circuit A1. An inverted value of the direction signal is applied to the AND circuit A2. Therefore, a clock signal for counting UP is outputted from an output end of the AND circuit A1, and a clock signal for counting DOWN is outputted from an output end of the AND circuit A2.

[0096] Fig. 24 shows an A/B phase conversion circuit for obtaining an A/B phase output by inputting the difference value to a programmable timer. When flip-flop circuits F1 and F2 output the logical value 0, the output of an exclusive OR circuit XO3 is 0. Accordingly, an input of an exclusive OR circuit XO1 is 1. If the input signal to a terminal T3 is 0, an output of an exclusive OR circuit XO1 becomes 1. Therefore, the clock signal is supplied to the flip-flop circuit F1 through the NAND circuit N1 while the gate signal is kept at 1.

[0097] The flip-flop circuit F1 is turned on according to the output of the NAND circuit N1, and the logical value 1 is

outputted to its output end Q. The exclusive OR circuit XO3 outputs 1, and the input to the exclusive OR circuit XO1 becomes 0. Therefore, the output of the exclusive OR circuit XO1 becomes 0, and the gate constructed by the NAND circuit N1 is closed. Further, the output of the exclusive OR circuit XO2 becomes 1 and the gate constructed by the NAND circuit N2 is opened to supply a clock signal to the flip-flop circuit F2.

[0098] When the flip-flop circuit F2 is turned on, the output of the exclusive OR circuit XO3 becomes 0. Therefore, the NAND circuit N1 is again opened and the NAND circuit N2 is closed. When the NAND circuit N1 is opened, a clock signal is supplied to the flip-flop circuit F1. Therefore, the flip-flop circuit F1 is inverted and the logical value is set to 0. The output of the exclusive OR circuit XO3 is set to 1, and therefore the NAND circuit N1 is again closed and the NAND circuit N2 is opened. Therefore, the flip-flop circuit F2 output a logical value 0 (and is returned to start.)

[0099] The above-mentioned operation is executed when the gate signal is 1. When the direction signal is 1, the flip-flop circuit F2 is first opened and then the flip-flop circuit F1 is opened. When the direction signal is 0, the flip-flop circuit Fl is first opened and then the flip-flop circuit F2 is opened.

[0100] When the gate signal is 0, both of the flip-flop circuits F1 and F2 are closed. Therefore, the flip-flop circuits F1 and F2 keep the previous condition.

[0101] Furthermore, if the output is A/B phase data, interpolation data in the look-up table can be constituted by converting the lower 2 bits of the obtained data into the Gray code. If the number of the interpolations is a multiple of 16, its 2 bits may be outputted as it is as A/B phase. That is, the correction circuit 107 may be omitted from the circuit in Fig. 9.

[0102] However, this method is theoretically concluded only in a case that the number of the interpolation data is the number of 4. Because the value of A/B phase is four values (00, 01, 10, 11) and therefore if the start of a cycle is 0, it is necessary that the end of the cycle must be 3.

[0103] Furthermore, since the look-up table for interpolation is constituted by one-fourth of one cycle data, it is necessary that if the start of the first quarter cycle is 0 the end of the fourth quarter cycle must be 3. Therefore, the number of the interpolation data must be a multiple of 16 (4 multiples of 4 values). However, if the number of interpolations to be executed is an odd multiple of 8 or an odd multiple of 4, it is easy to execute such an interpolation by applying a correction as shown in Fig. 10.

[0104] In Fig. 10, A denotes a signal of phase A, B denotes a signal of phase B, a denotes an interpolation signal of phase A in the quadrant I, and b denotes an interpolation signal of phase B in the quadrant I. Further, 16n, 8(2n-1) and 4(2n-1) denote that the number of the interpolation is respectively a multiple of 16, an odd multiple of 8 and an odd multiple of 4. $\bar{a}$ and $\bar{b}$ (with the "-" above the letter) indicates an inverse number (complement). Fig. 21 shows a circuit for executing the interpolation data whose number is an odd multiple of 4. This circuit executes conversion so as to satisfy the truth table of Fig. 10.

[0105] Fig. 12 shows a waveform graph for explaining the above mentioned contents for the case that the number of interpolations is an odd multiple of 4 (12 distribution 4 x 3=12). The upper two waves show desired wave forms of phase A and phase B. The intermediate two waves show wave forms read from the ROM for the look-up table. The lower two waves show corrected waves of phase A and phase B. The lower two waves shown in Fig. 12 are constituted by first to fourth sections divided by a broken line. In the first section positioned at the left hand side on Fig. 12, the sine and cosine waves are represented by the data from the look-up table as it is. In the second section, the phase A signal is replaced by the previous phase B signal, and the phase B signal is replaced by the inverted value of the previous phase A signal. In the third section, the phase A signal is replaced by the phase B signal at the second section, that is, by the inverted value of the phase A signal at the first section, and the phase B signal is replaced by the inverted value of the previous phase A signal. In the fourth section positioned at the right hand side, the phase A signal is replaced by the inverted value of the previous phase B signal, and the phase B signal is replaced by the inverted value of the previous phase A signal.

[0106] With these corrections of the signals, a desired waveform, which indicates a 50% duty, is obtained.

[0107] Fig. 13 shows waveforms for the case where one cycle is split into $24 = 8 \times 3$ which is of an odd multiple of 8. The upper two waveforms denote desired waveforms. The intermediate two waveforms denote waveforms which are simply constituted by the data from the look-up table in the ROM. The lower two waveforms denote corrected waveforms of the intermediate two wave forms by inverting the previous self value at every section.

[0108] Although the above-mentioned decision of the data for each quadrant and the exchange of the data appear like complicated operations, the logic circuit for executing the above-mentioned operations can be constituted by simple AND-OR structure as shown in Figs. 20 and 21 and therefore, it is easy to increase the processing speed.

Claims

1. An interpolation device for interpolating at least one cyclic analog signals, the cyclic analog signal periodically changing its amplitude corresponding to a position function of a displacement, the interpolation device comprising:

an analog-digital converter (1) converting the analog signal to a digital signal; and

an interpolating means (3) for interpolating an input to said interpolating means (3);

characterized by

a digital filter (2) for removing a high-frequency component of said digital signal; and by

a hysteresis circuit (4) which is disposed between said digital filter and said interpolating means (3).

2. An interpolation device as claimed in claim 1, wherein said digital filter is constituted by a microcomputer.

3. The interpolation device according to claim 1 or 2, wherein said hysteresis circuit (4) comprises:

data storage means for storing a present data value and a previous data value;

means for determining whether said present data value is smaller than said previous data value;

means for determining whether said present data value is larger than the sum of said previous data value and a hysteresis value, if said present data value is not smaller than said previous data value;

means for subtracting said hysteresis value from said present data value if said present data value is larger than said sum;

means for storing said present data value or said present data value minus the hysteresis value in said storage means for storing said previous data.

4. An interpolation device as claimed in claims 2 or 3, wherein said digital filter and said hysteresis circuit are constituted by a microcomputer.

5. An interpolation device as claimed in any of claims 1 to 4, where two analog signals that are shifted in phase by 90° are to be interpolated said interpolating means including a look-up table (108, 205) for storing interpolation data corresponding to one of the four quadrants of a Lissajous figure formed at a time when the analog signals are disposed on an x-y plane, and a quadrant converting means (107, 204) for obtaining interpolation data of the other quadrants by utilizing said data stored in said look-up table (108, 205).

6. An interpolation device as claimed in claim 5, wherein said quadrant converting means (107, 204) executes a quadrant conversion of the data in the look-up table (108, 205) such that the logical value of the most significant bit or reference bit of each of the digital signals is detected and a part of the digital signal except for the most significant bit or reference bit is inverted or not inverted and exchanged according to the detected logical value.

7. An interpolation device as claimed in claim 6, wherein interpolation data stored in the look-up table (108, 205) comprises 2 bit gray-code signals of a small cycle which is obtained by splitting the cycle of the supplied analog signal into a multiple of 16.

8. An interpolation device as claimed in claim 6, wherein interpolation data stored in the look-up table (108, 205) comprises 2 bit gray-code signals of a small cycle which is obtained by splitting the cycle of the supplied analog signal into an odd multiple of 8, said quadrant converting means (107, 204) executing a read out control of the look-up table (108, 205) so that the 2 bit gray-code signal is inverted and outputted when the interpolation is executed relative to the adjacent quadrant of that of the look-up table (108, 205).

9. An interpolation device as claimed in claim 6, wherein interpolation data stored in the look-up table comprises 2 bit gray-code signals of a small cycle which is obtained by splitting the cycle of the supplied analog signal into an odd multiple of 4, said quadrant converting means (107, 204) executing a read out control of the look-up table (108, 205) so that one of the 2 bit gray-code signals of phase A and phase B is replaced by the previous value of the other 2 bit gray-code signal and the other 2 bit gray-code signal is replaced by the previous inversion signal of the 2 bit gray-code signal when the interpolation is executed relative to the adjacent quadrant of the look-up table (108, 205).

10. An interpolation device as claimed in claim 6, wherein interpolation data stored in the look-up table (108, 205) comprises three sets of data of 2 bit gray-code signals of a small cycle which are obtained by splitting the cycle of the supplied analog signal into a multiple of 16, into an odd multiple of 8 and into an odd multiple of 4, said quadrant converting means comprising means for executing a read out control of the look-up table so that the 2 bit gray-code signal is inverted and outputted when the interpolation is executed relative to the adjacent quadrant of that of the look-up table.

11. An interpolation device as claimed in claim 6, wherein said interpolating means includes an adder (206) which adds an offset value (1/4, 1/2 and 3/4) of a split number to the data obtained from the look-up table (205) according to the position of the quadrants.

12. An interpolation device as claimed in claim 11, said interpolating means further comprising a difference value generating section (321 to 335) for obtaining a difference between a previous value and a present value of the output of the adder (206) while the output of the adder is held by each sampling.

13. An interpolation device as claimed in claim 12, wherein said interpolating means further comprises an A/B phase converter which converts the output data of the difference value generating section into a two-phase pulse train.

Patentansprüche

1. Interpolationsvorrichtung zum Interpolieren von zumindest einem zyklischen analogen Signal, wobei das zyklische analoge Signal periodisch seine Amplitude ändert gemäß einer Positionsfunktion von einer Verschiebung, die Interpolationsvorrichtung aufweisend:

einen analog-zu-digital Umwandler (1), der das analoge Signal in ein digitales Signal umwandelt; und

eine interpolierende Einrichtung (3) zum Interpolieren einer Eingabe dieser interpolierenden Einrichtung (3);

gekennzeichnet durch

ein digitales Filter (2) zum Entfernen einer Hochfrequenzkomponente des digitalen Signals; und durch

einen Hysterese-Schaltkreis (4), der zwischen dem digitalen Filter und der interpolierenden Einrichtung (3) angeordnet ist.

2. Interpolationsvorrichtung nach Anspruch 1, wobei das digitale Filter durch einen Mikrocomputer ausgebildet ist.

3. Interpolationsvorrichtung nach Anspruch 1 oder 2, wobei der Hysterese-Schaltkreis (4) aufweist:

eine Datenspeichereinrichtung zum Speichern eines gegenwärtigen Datenwerts und eines vorangegangenen Datenwerts;

eine Einrichtung zum Bestimmen, ob der gegenwärtige Datenwert kleiner ist als der vorangegangene Datenwert;

eine Einrichtung zum Bestimmen, ob der gegenwärtige Datenwert größer ist als die Summe aus dem vorangegangenen Datenwert und einem Hysterese-Wert, falls der gegenwärtige Datenwert nicht kleiner ist als der vorangegangene Datenwert;

eine Einrichtung zum Subtrahieren des Hysterese-Werts von dem gegenwärtigen Datenwert, falls der gegenwärtige Datenwert größer ist als die Summe;

eine Einrichtung zum Speichern des gegenwärtigen Datenwerts oder des gegenwärtigen Datenwerts minus dem Hysterese-Wert in der Speichereinrichtung zum Speichern der vorangegangenen Daten.

4. Interpolationsvorrichtung nach Anspruch 2 oder 3, wobei das digitale Filter und der Hysterese-Schaltkreis durch einen Mikrocomputer ausgebildet sind.

5. Interpolationsvorrichtung nach einem der Ansprüche 1 bis 4, wobei zwei analoge Signale, die in ihrer Phase um 90° verschoben sind, interpoliert werden, die interpolierende Einrichtung eine Nachschlagtabelle (108, 205) aufweist zum Speichern von Interpolationsdaten gemäß einem der vier Quadranten einer Lissajous-Figur, die zu einem Zeitpunkt gebildet wird, wenn die analogen Signale auf einer x-y-Ebene abgebildet werden, und eine Quadrantumwandlungseinrichtung (107, 204) zum Bestimmen von Interpolationsdaten der anderen Quadranten durch Verwenden der Daten, die in der Nachschlagtabelle (108, 205) gespeichert sind.

6. Interpolationsvorrichtung nach Anspruch 5, wobei die Quadrantumwandlungseinrichtung (107, 204) eine Quadrantumwandlung der Daten in der Nachschlagtabelle (108, 205) ausführt, so dass der logische Wert des höchstwertigen Bits oder Referenzbits jedes der digitalen Signale erfasst wird und ein Teil des digitalen Signals mit Ausnahme des höchstwertigen Bits oder Referenzbits invertiert wird oder nicht invertiert und ausgetauscht wird gemäß dem erfassten logischen Wert.

7. Interpolationsvorrichtung nach Anspruch 6, wobei Interpolationsdaten, die in der Nachschlagtabelle (108, 205) gespeichert sind, 2 Bit Gray-Code-Signale eines kleinen Zykluses aufweisen, die bestimmt werden durch Aufsplittern des Zykluses des zugeführten analogen Signals in ein Vielfaches von 16.

8. Interpolationsvorrichtung nach Anspruch 6, wobei Interpolationsdaten, die in der Nachschlagtabelle (108, 205) gespeichert sind, 2 Bit Gray-Code-Signale eines kleines Zykluses aufweisen, die bestimmt werden durch Aufsplittern des Zykluses des zugeführten analogen Signals in ein ungerades Vielfaches von 8, die Quadrantumwandlungseinrichtung (107, 204) eine Auslesesteuerung der Nachschlagtabelle (108, 205) ausführt, so dass das 2 Bit Gray-Code-Signal invertiert wird und ausgegeben wird, wenn die Interpolation ausgeführt wird in Bezug auf den benachbarten Quadranten zu dem der Nachschlagtabelle (108, 205).

9. Interpolationsvorrichtung nach Anspruch 6, wobei Interpolationsdaten, die in der Nachschlagtabelle gespeichert sind, 2 Bit Gray-Code-Signale eines kleinen Zykluses aufweisen, die bestimmt werden durch Aufsplittern des Zykluses des zugeführten analogen Signals in ein ungerades Vielfaches von 4, die Quadrantumwandlungseinrichtung (107, 204) eine Auslesesteuerung der Nachschlagtabelle (108, 205) ausführt, so dass eines der 2 Bit Gray-Code-Signale mit einer Phase A und einer Phase B ersetzt wird durch den vorangegangenen Wert des anderen 2 Bit Gray-Code-Signals und das andere 2 Bit Gray-Code-Signal wird ersetzt durch das vorangegangene Invertierungssignal des 2 Bit Gray-Code-Signals wenn die Interpolation ausgeführt wird in Bezug auf den benachbarten Quadranten der Nachschlagtabelle (108, 205).

10. Interpolationsvorrichtung nach Anspruch 6, wobei Interpolationsdaten, die in der Nachschlagtabelle (108, 205) gespeichert sind, drei Sätze von Daten von 2 Bit Gray-Code-Signalen eines kleinen Zykluses aufweisen, die bestimmt werden durch Aufsplittern des Zykluses des zugeführten analogen Signals in ein Vielfaches von 16, in ein ungerades Vielfaches von 8 und in ein ungerades Vielfaches von 4, die Quadrantumwandlungseinrichtung eine Einrichtung aufweist zum Ausführen einer Auslesesteuerung der Nachschlagtabelle, so dass das 2 Bit Gray-Code-Signal invertiert wird und ausgegeben wird, wenn die Interpolation ausgeführt wird in Bezug auf den benachbarten Quadranten zu dem der Nachschlagtabelle.

11. Interpolationsvorrichtung nach Anspruch 6, wobei die interpolierende Einrichtung einen Addierer (206) aufweist, der einen Offset-Wert (1/4, 1/2 und 3/4) einer Aufsplittanzahl zu den Daten hinzuaddiert, die von der Nachschlagtabelle (205) erhalten werden gemäß der Position der Quadranten.

12. Interpolationsvorrichtung nach Anspruch 11, wobei die interpolierende Einrichtung des Weiteren aufweist eine Differenzwerterzeugungseinrichtung (321 bis 335) zum Bestimmen einer Differenz zwischen einem vorangegangenen Wert und einem gegenwärtigen Wert der Ausgabe des Addierers (206), während die Ausgabe des Addierers bei jedem Abtasten gehalten wird.

13. Interpolationsvorrichtung nach Anspruch 12, wobei die interpolierende Einrichtung des Weiteren aufweist einen A/B-Phasenumwandler, der die Ausgabedaten der Differenzwerterzeugungseinrichtung umwandelt in eine Zwei-Phasen-Impulsfolge.

Revendications

1. Dispositif d'interpolation pour interpoler au moins un signal analogique cyclique, le signal analogique cyclique

changeant périodiquement son amplitude correspondant à une fonction de position d'un déplacement, le dispositif d'interpolation comprenant :

un convertisseur analogique-numérique (1) convertissant le signal analogique en signal numérique ; et un moyen d'interpolation (3) pour interpoler une entrée audit moyen d'interpolation (3) ;

caractérisé par

un filtre numérique (2) pour supprimer une composante haute fréquence dudit signal numérique ; et par un circuit d'hystérésis (4) qui est disposé entre ledit filtre numérique et ledit moyen d'interpolation (3).

2. Dispositif d'interpolation selon la revendication 1, où ledit filtre numérique est constitué par un micro-ordinateur.

3. Dispositif d'interpolation selon la revendication 1 ou 2, où ledit circuit d'hystérésis (4) comprend :

un moyen de stockage de données pour stocker une valeur de donnée présente et une valeur de donnée précédente ;
un moyen pour déterminer si ladite valeur de donnée présente est plus petite que ladite valeur de donnée précédente ; ,
un moyen pour déterminer si ladite valeur de donnée présente est plus grande que la somme de ladite valeur de donnée précédente et une valeur d'hystérésis, si ladite valeur de donnée présente n'est pas plus petite que ladite valeur de donnée précédente ;
un moyen pour soustraire ladite valeur d'hystérésis de ladite valeur de donnée présente si ladite valeur de donnée présente est plus grande que ladite somme ;
un moyen pour stocker ladite valeur de donnée présente ou ladite valeur de donnée présente moins la valeur d'hystérésis dans ledit moyen de stockage pour stocker ladite donnée précédente.

4. Dispositif d'interpolation selon la revendication 2 ou 3, où ledit filtre numérique et ledit circuit d'hystérésis sont constitués par un micro-ordinateur.

5. Dispositif d'interpolation selon l'une des revendications 1 à 4, où deux signaux analogiques qui sont décalés en phase de 90° doivent être interpolés, ledit moyen d'interpolation incluant une table à consulter (108, 205) pour stocker des données d'interpolation correspondant à l'un de quatre quadrants d'une figure de Lissajous formée à un moment où les signaux analogiques sont disposés sur un plan x-y, et un moyen de conversion de quadrant (107, 204) pour obtenir des données d'interpolation des autres quadrants en utilisant lesdites données stockées dans ladite table à consulter (108, 205).

6. Dispositif d'interpolation selon la revendication 5, où ledit moyen de conversion de quadrant (107, 204) exécute une conversion des quadrants des données dans la table à consulter (108, 205) de telle sorte que la valeur logique de l'élément binaire le plus important ou de l'élément binaire de référence de chacun des signaux numériques est détectée et qu'une partie du signal numérique à l'exception de l'élément binaire le plus important ou de l'élément binaire de référence est inversée ou non inversée et échangée en accord avec la valeur logique détectée.

7. Dispositif d'interpolation selon la revendication 6, où les données d'interpolation stockées dans la table à consulter (108, 205) comprennent des signaux de code de Gray à 2 éléments binaires d'un petit cycle qui est obtenu en divisant le cycle du signal analogique fourni en un multiple de 16.

8. Dispositif d'interpolation selon la revendication 6, où les données d'interpolation stockées dans la table à consulter (108, 205) comprennent des signaux de code de Gray à 2 éléments binaires d'un petit cycle qui est obtenu en divisant le cycle du signal analogique fourni en un multiple impair de 8, ledit moyen de conversion de quadrant (107, 204), exécutant un contrôle de lecture de la table à consulter (108, 205) de telle sorte que le signal de code de Gray à 2 éléments binaires est inversé et émis lorsque l'interpolation est exécutée relativement au quadrant adjacent à celui de la table à consulter (108, 205).

9. Dispositif d'interpolation selon la revendication 6, où les données d'interpolation stockées dans la table à consulter comprennent des signaux de code de Gray à 2 éléments binaires d'un petit cycle qui est obtenu en divisant le cycle du signal analogique fourni en un multiple impair de 4, ledit moyen de conversion de quadrant (107, 204) exécutant un contrôle de lecture de la table à consulter (108, 205) de telle sorte que l'un des signaux de code de

Gray à 2 éléments binaires de la phase A et de la phase B soit remplacé par la valeur précédente de l'autre signal de code de Gray à 2 éléments binaires, et l'autre signal de code de Gray à 2 éléments binaires est remplacé par le signal d'inversion précédent du signal de code de Gray à 2 éléments binaires lorsque l'interpolation est exécutée relativement au quadrant adjacent de la table à consulter (108, 205).

10. Dispositif d'interpolation selon la revendication 6, où les données d'interpolation stockées dans la table à consulter (108, 205) comprennent trois ensembles de données de signaux de code de Gray à 2 éléments binaires d'un petit cycle qui sont obtenus en divisant le cycle du signal analogique fourni en un multiple de 16, en un multiple impair de 8 et en un multiple impair de 4, ledit moyen de conversion de quadrant comprenant un moyen pour exécuter un contrôle de lecture de la table à consulter de telle sorte que le signal de code de Gray à 2 éléments binaires est inversé et émis lorsque l'interpolation est exécutée relativement au quadrant adjacent à celui de la table à consulter.

11. Dispositif d'interpolation selon la revendication 6, où ledit moyen d'interpolation comporte un additionneur (206) qui ajoute une valeur de décalage (1/4, 1/2 et 3/4) d'un nombre divisé aux données obtenues de la table à consulter (205) selon la position des quadrants.

12. Dispositif d'interpolation selon la revendication 11, où ledit moyen d'interpolation comprend en outre une section de génération de valeurs de différence (321 à 335) pour obtenir une différence entre une valeur précédente et une valeur présente de la sortie de l'additionneur (206) pendant que la sortie de l'additionneur est maintenue par chaque échantillonnage.

13. Dispositif d'interpolation selon la revendication 12, où ledit moyen d'interpolation comprend en outre un convertisseur de phase A/B qui convertit les données sorties de la section de génération de valeurs de différence en un train d'impulsions à deux phases.

FIG.1

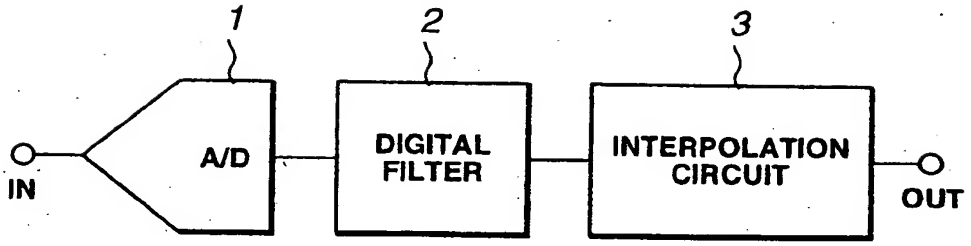


FIG.2

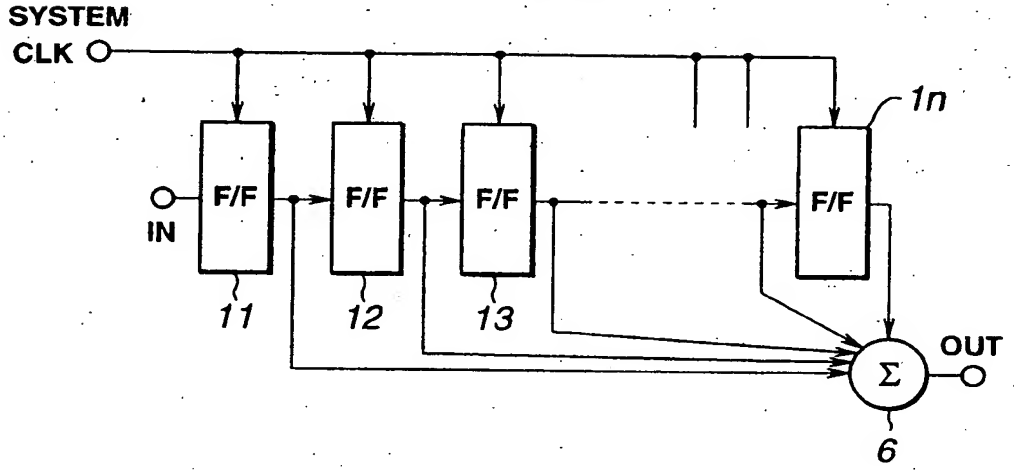


FIG.3

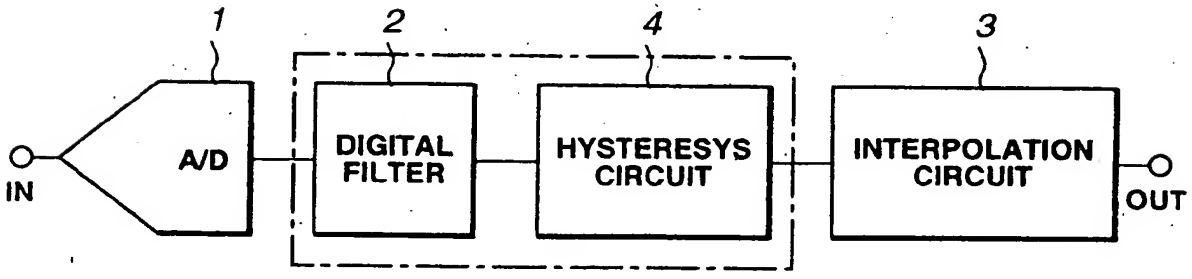


FIG.4

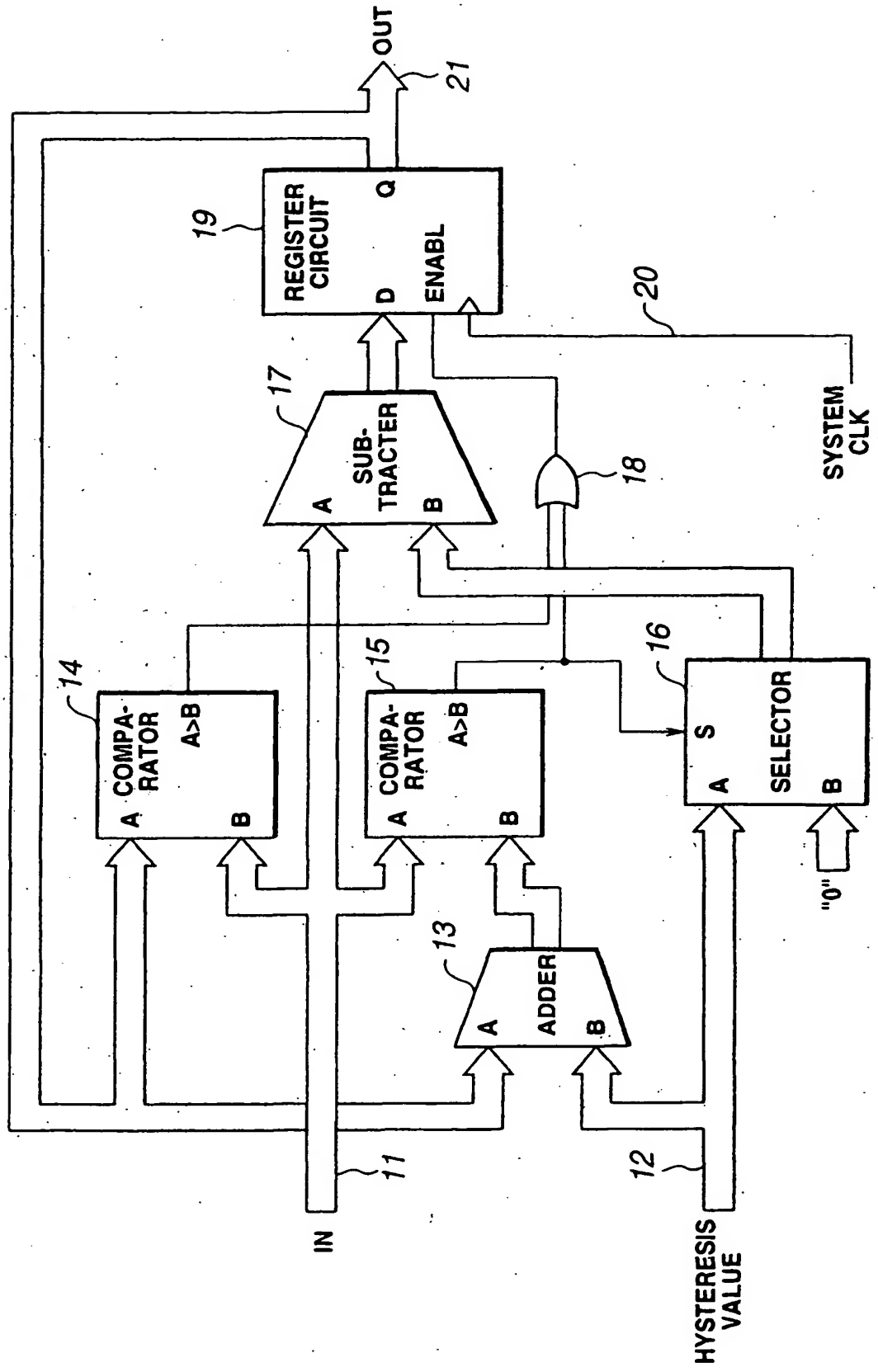

OUT
21
19
REGISTER CIRCUIT
Q
D
ENABL
20
SYSTEM CLK
17
SUB-TRACTER
A
B
18
14
COMPA-RATOR
A>B
A
B
15
COMPA-RATOR
A>B
A
B
16
SELECTOR
S
A
B
"0"
13
ADDER
A
B
IN
11
12
HYSTERESIS VALUE

FIG.5

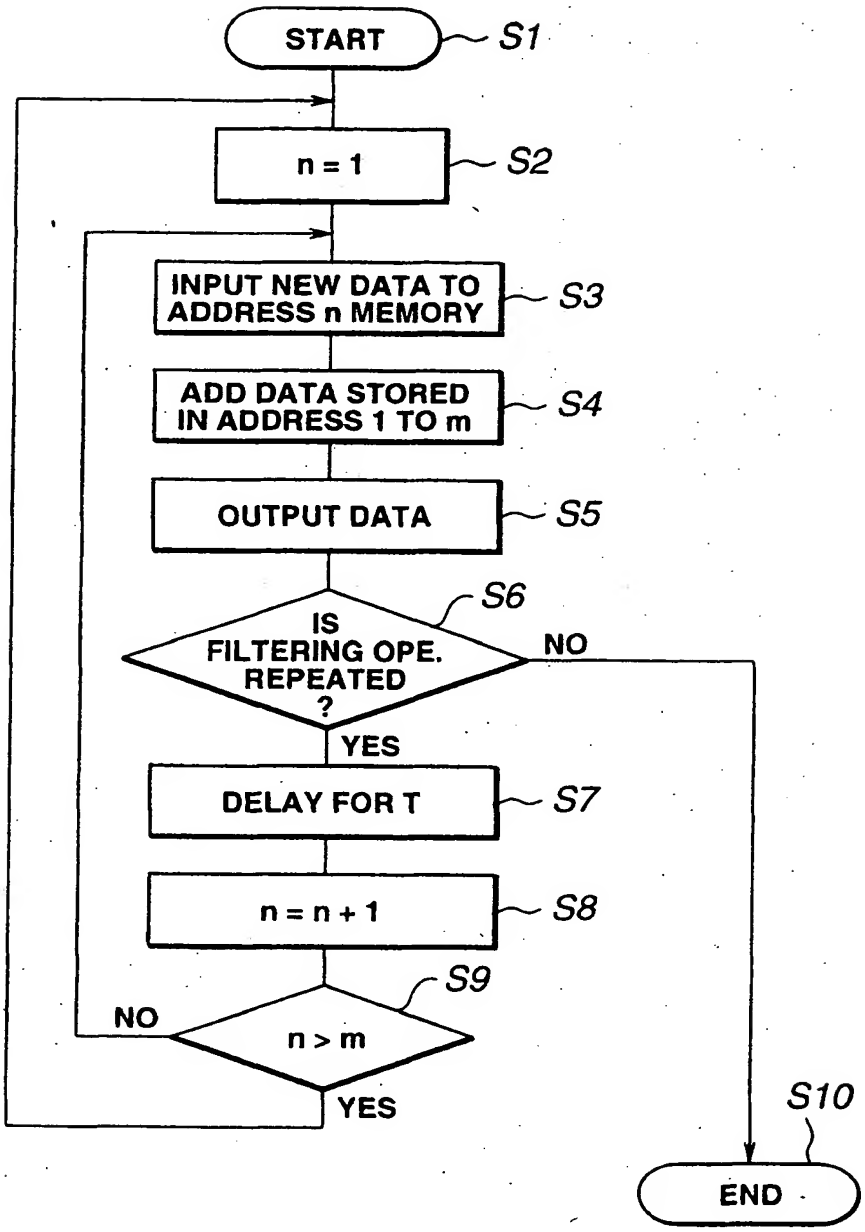

START
S1
n = 1
S2
INPUT NEW DATA TO ADDRESS n MEMORY
S3
ADD DATA STORED IN ADDRESS 1 TO m
S4
OUTPUT DATA
S5
S6
IS FILTERING OPE. REPEATED ?
NO
YES
DELAY FOR T
S7
n = n + 1
S8
S9
NO
n > m
YES
S10
END

FIG.6

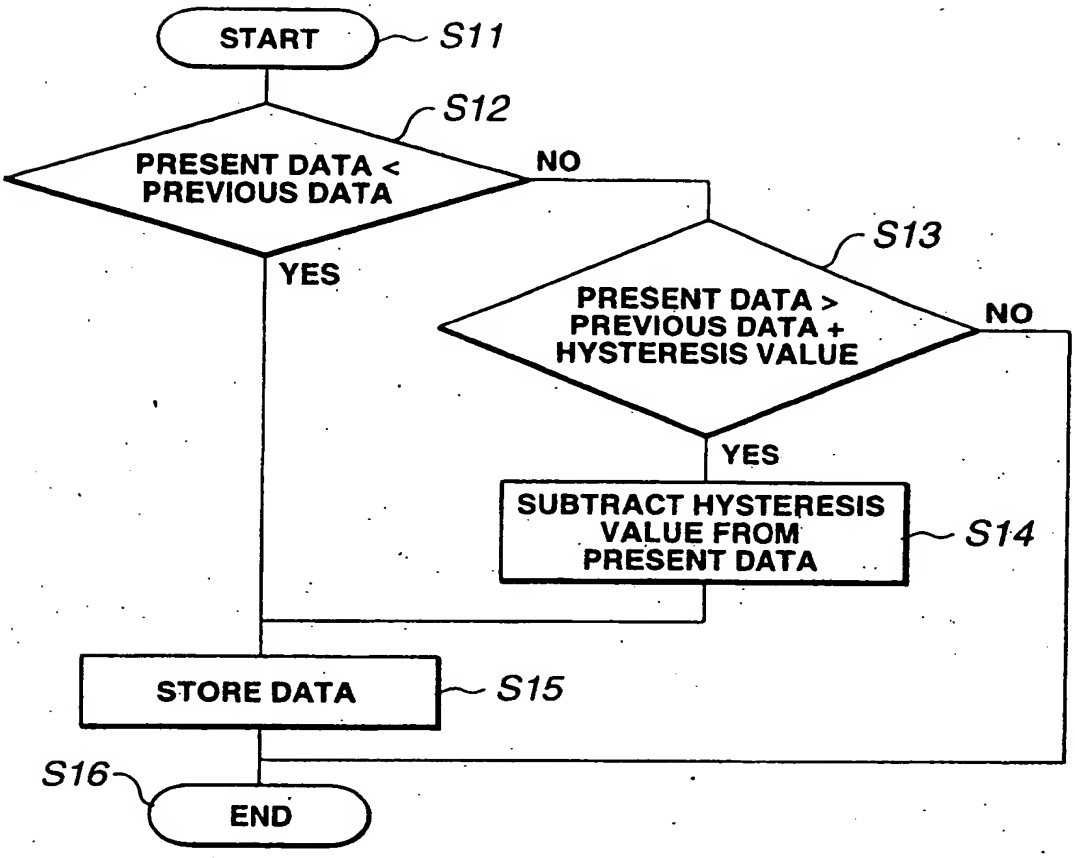

START
S11
S12
PRESENT DATA < PREVIOUS DATA
NO
YES
S13
PRESENT DATA > PREVIOUS DATA + HYSTERESIS VALUE
NO
YES
SUBTRACT HYSTERESIS VALUE FROM PRESENT DATA
S14
STORE DATA
S15
S16
END

FIG.7

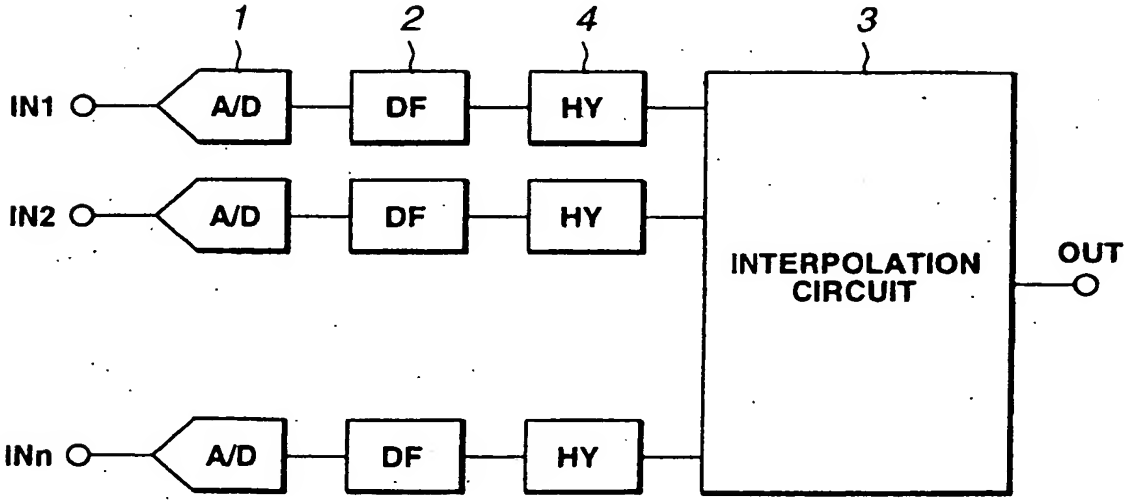

1
2
4
3
IN1
A/D
DF
HY
IN2
A/D
DF
HY
INn
A/D
DF
HY
INTERPOLATION CIRCUIT
OUT

FIG.8

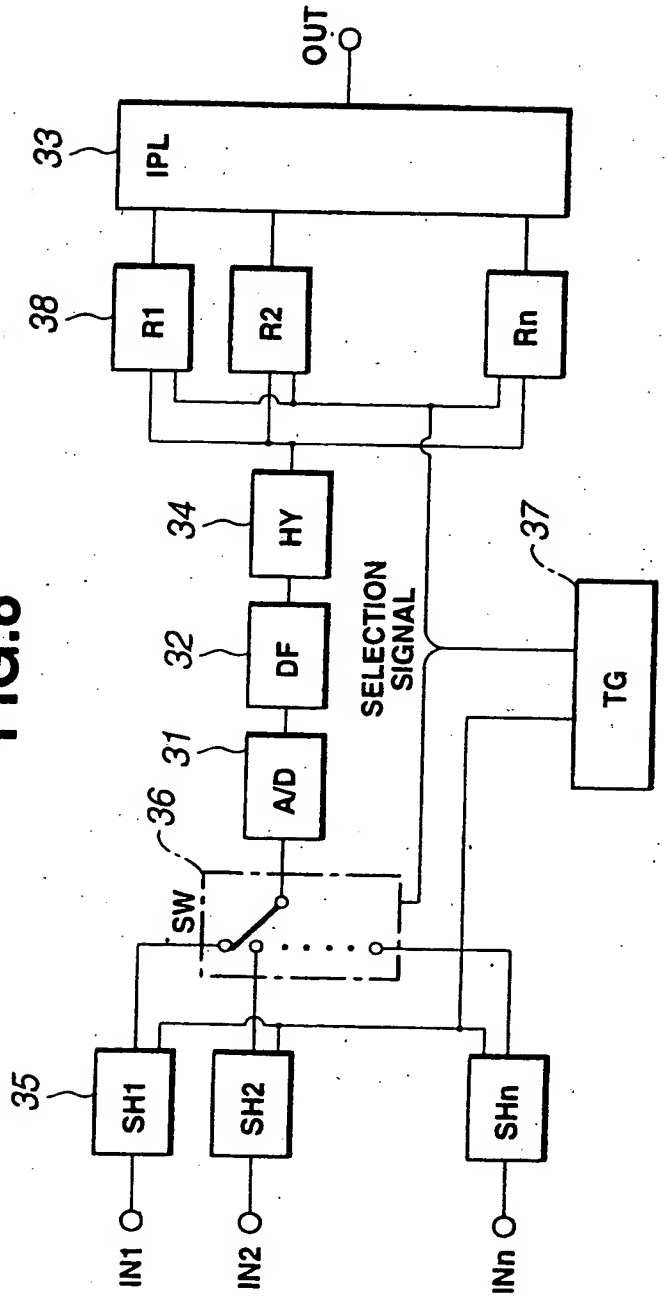

OUT
33
IPL
38
R1
R2
Rn
34
HY
32
DF
31
A/D
36
SW
37
TG
SELECTION SIGNAL
35
SH1
SH2
SHn
IN1
IN2
INn

FIG.9

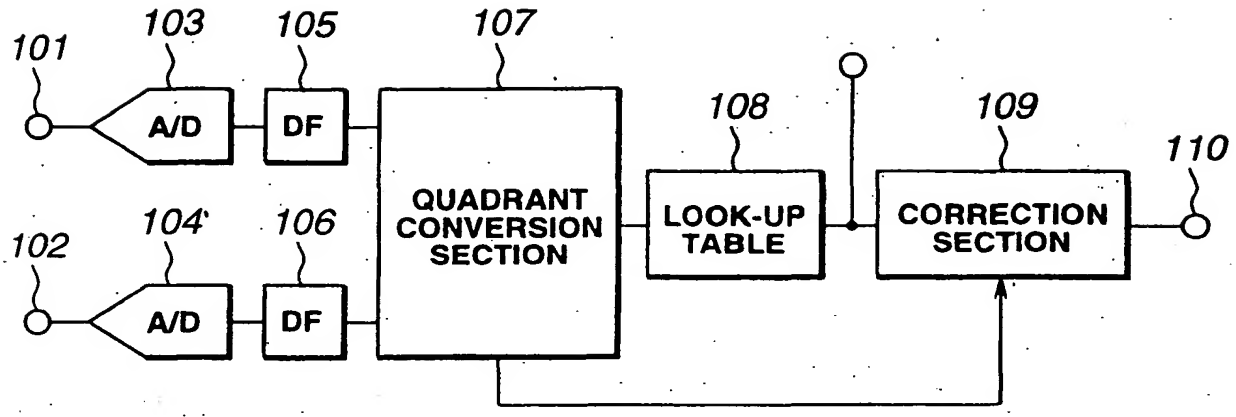


FIG.10

SPILIT NUMBER	16n		8(2n-1)		4(2n-1)	
OUTPUT	A	B	A	B	A	B
QUADRANT I	a	b	a	b	a	b
QUADRANT II	a	b	$\bar{a}$	$\bar{b}$	b	$\bar{a}$
QUADRANT III	a	b	a	b	$\bar{a}$	$\bar{b}$
QUADRANT IV	a	b	$\bar{a}$	$\bar{b}$	$\bar{b}$	a

FIG.11

TRUTH TABLE MSB

QUADRANT	SC	LOWER ADDRESS	UPPER ADDRESS
I	11	SIN	COS
II	10	$\overline{\text{COS}}$	SIN
III	00	$\overline{\text{SIN}}$	$\overline{\text{COS}}$
IV	01	COS	$\overline{\text{SIN}}$

TABLE 1

FIG.12

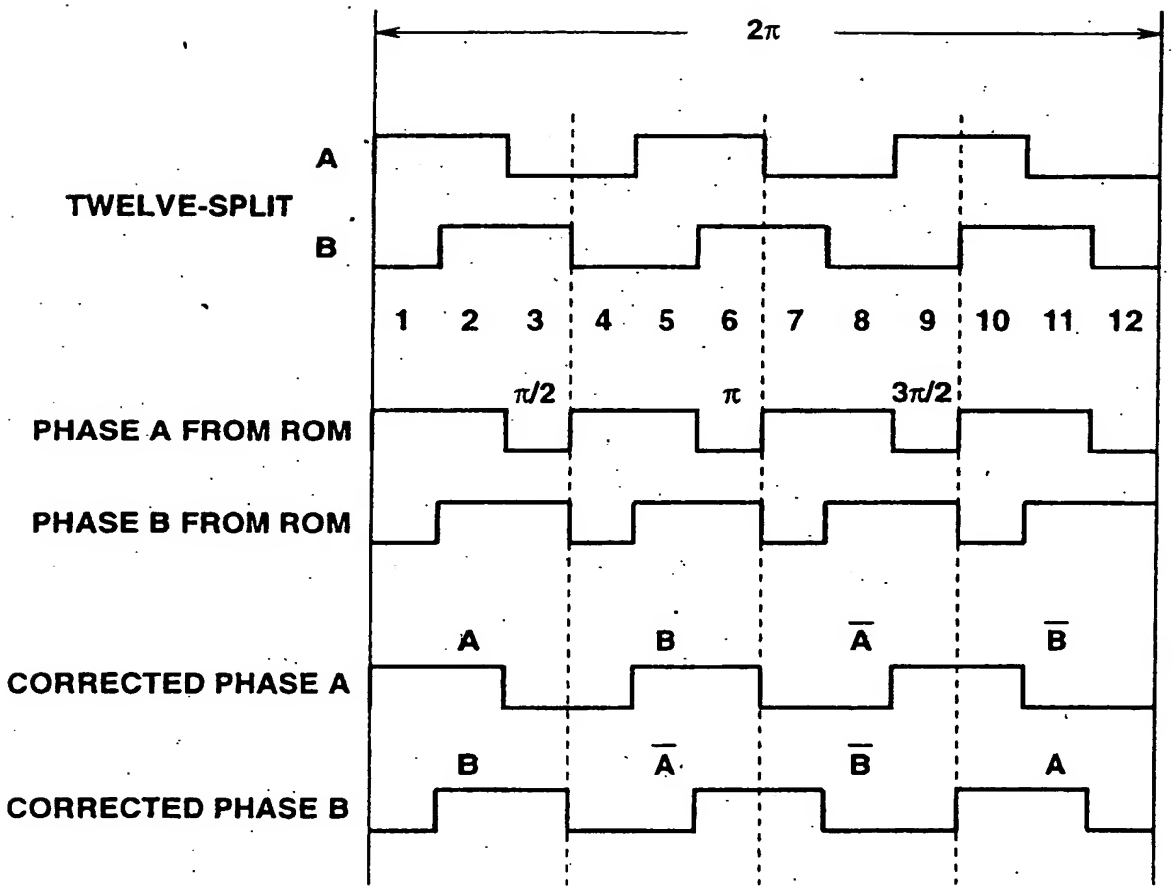

2π
A
TWELVE-SPLIT
B
1 2 3 4 5 6 7 8 9 10 11 12
π/2
π
3π/2
PHASE A FROM ROM
PHASE B FROM ROM
A
B
Ā
B̄
CORRECTED PHASE A
B
Ā
B̄
A
CORRECTED PHASE B

FIG.13

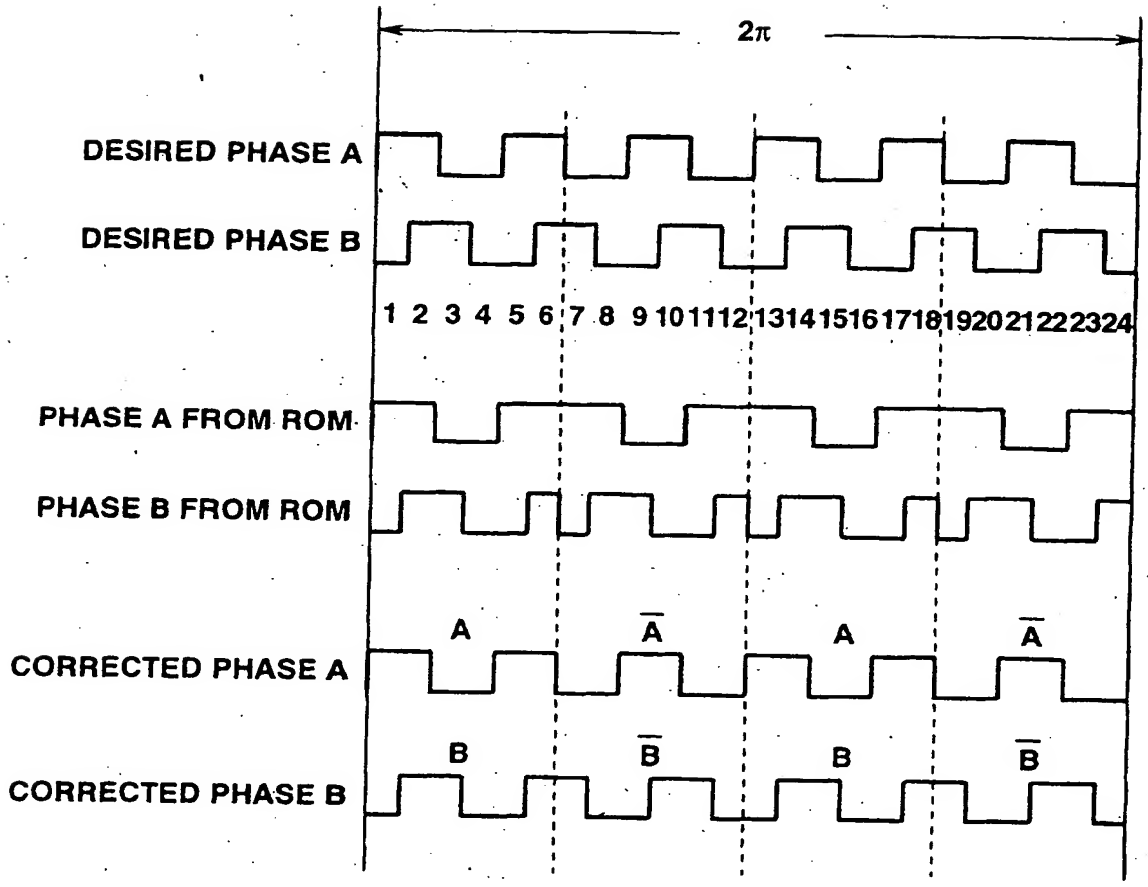

2π
DESIRED PHASE A
DESIRED PHASE B
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
PHASE A FROM ROM
PHASE B FROM ROM
CORRECTED PHASE A
A
Ā
A
Ā
CORRECTED PHASE B
B
B̄
B
B̄

FIG.14

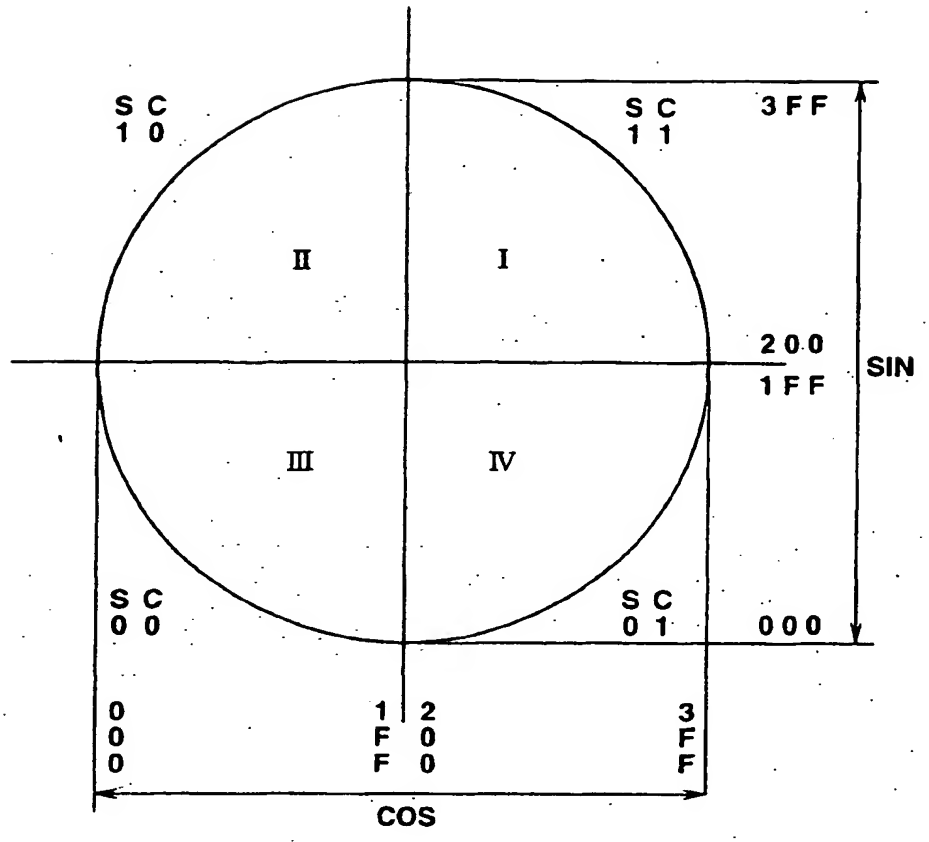

S C
1 0
S C
1 1
3 F F
II
I
2 0 0
1 F F
SIN
III
IV
S C
0 0
S C
0 1
0 0 0
0
0
0
1
F
F
2
0
0
3
F
F
COS

FIG.15

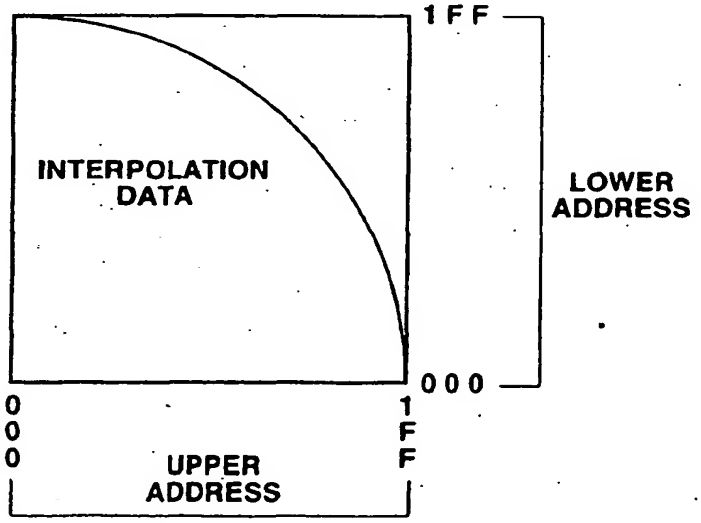

1 F F
INTERPOLATION
DATA
LOWER
ADDRESS
0 0 0
0
0
0
1
F
F
UPPER
ADDRESS

FIG.16

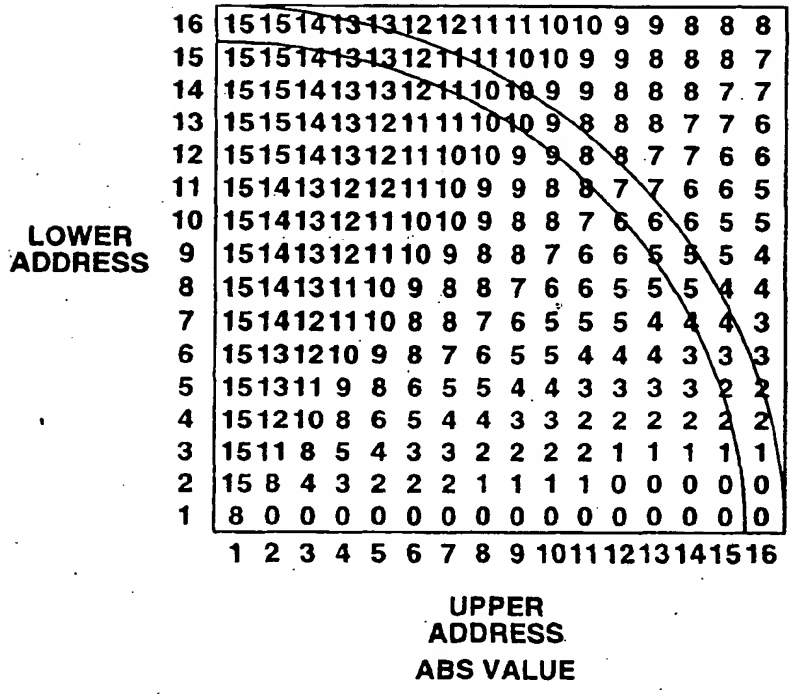

LOWER ADDRESS
16 15 15 14 13 13 12 12 11 11 10 10 9 9 8 8 8
15 15 15 14 13 13 12 11 11 10 10 9 9 8 8 8 7
14 15 15 14 13 13 12 11 10 10 9 9 8 8 8 7 7
13 15 15 14 13 12 11 11 10 10 9 8 8 8 7 7 6
12 15 15 14 13 12 11 10 10 9 9 8 8 7 7 6 6
11 15 14 13 12 12 11 10 9 9 8 8 7 7 6 6 5
10 15 14 13 12 11 10 10 9 8 8 7 6 6 6 5 5
9 15 14 13 12 11 10 9 8 8 7 6 6 5 5 5 4
8 15 14 13 11 10 9 8 8 7 6 6 5 5 5 4 4
7 15 14 12 11 10 8 8 7 6 5 5 5 4 4 4 3
6 15 13 12 10 9 8 7 6 5 5 4 4 4 3 3 3
5 15 13 11 9 8 6 5 5 4 4 3 3 3 3 2 2
4 15 12 10 8 6 5 4 4 3 3 2 2 2 2 2 2
3 15 11 8 5 4 3 3 2 2 2 2 1 1 1 1 1
2 15 8 4 3 2 2 2 1 1 1 1 0 0 0 0 0
1 8 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
UPPER ADDRESS
ABS VALUE

FIG.17

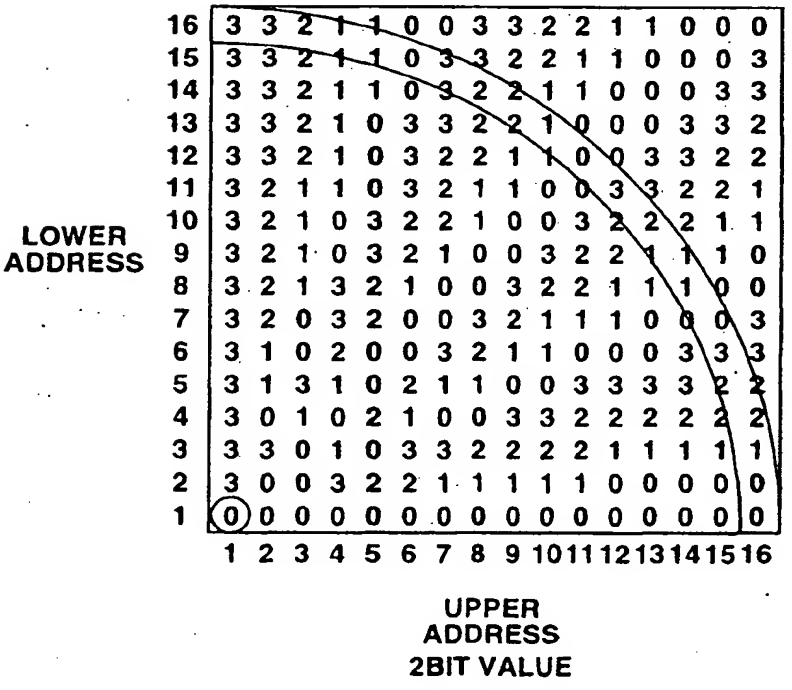

LOWER ADDRESS
16 3 3 2 1 1 0 0 3 3 2 2 1 1 0 0 0
15 3 3 2 1 1 0 3 3 2 2 1 1 0 0 0 3
14 3 3 2 1 1 0 3 2 2 1 1 0 0 0 3 3
13 3 3 2 1 0 3 3 2 2 1 0 0 0 3 3 2
12 3 3 2 1 0 3 2 2 1 1 0 0 3 3 2 2
11 3 2 1 1 0 3 2 1 1 0 0 3 3 2 2 1
10 3 2 1 0 3 2 2 1 0 0 3 2 2 2 1 1
9 3 2 1 0 3 2 1 0 0 3 2 2 1 1 1 0
8 3 2 1 3 2 1 0 0 3 2 2 1 1 1 0 0
7 3 2 0 3 2 0 0 3 2 1 1 1 0 0 0 3
6 3 1 0 2 0 0 3 2 1 1 0 0 0 3 3 3
5 3 1 3 1 0 2 1 1 0 0 3 3 3 3 2 2
4 3 0 1 0 2 1 0 0 3 3 2 2 2 2 2 2
3 3 3 0 1 0 3 3 2 2 2 2 1 1 1 1 1
2 3 0 0 3 2 2 1 1 1 1 1 0 0 0 0 0
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
UPPER ADDRESS
2BIT VALUE

FIG.18A

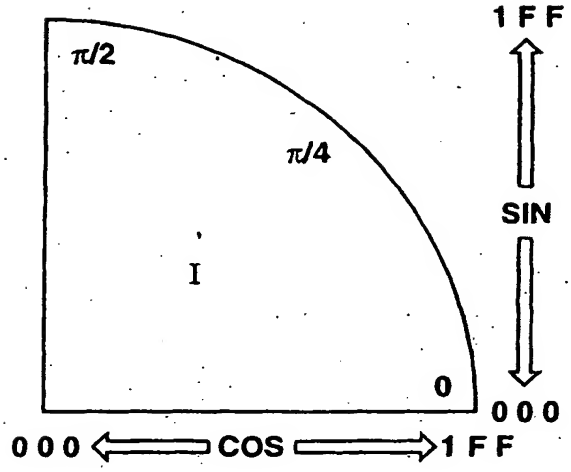


FIG.18B

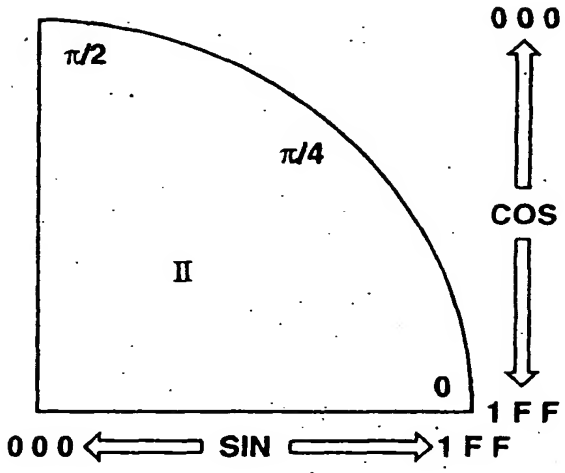


FIG.18C

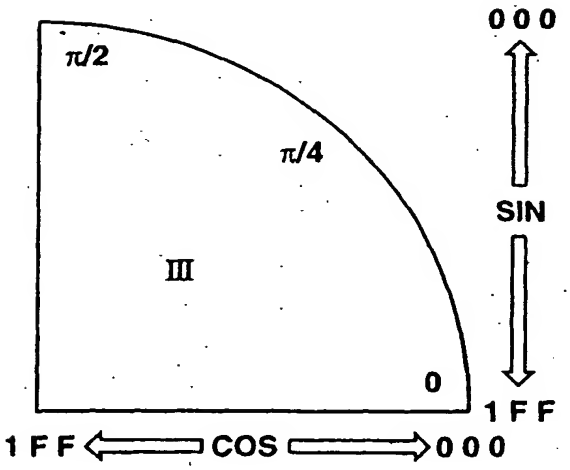


FIG.18D

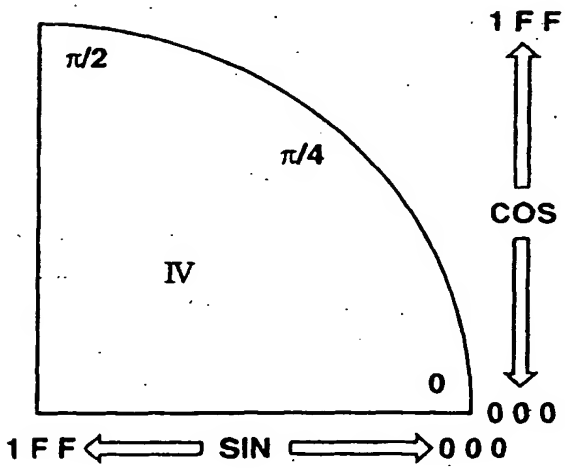


FIG.19

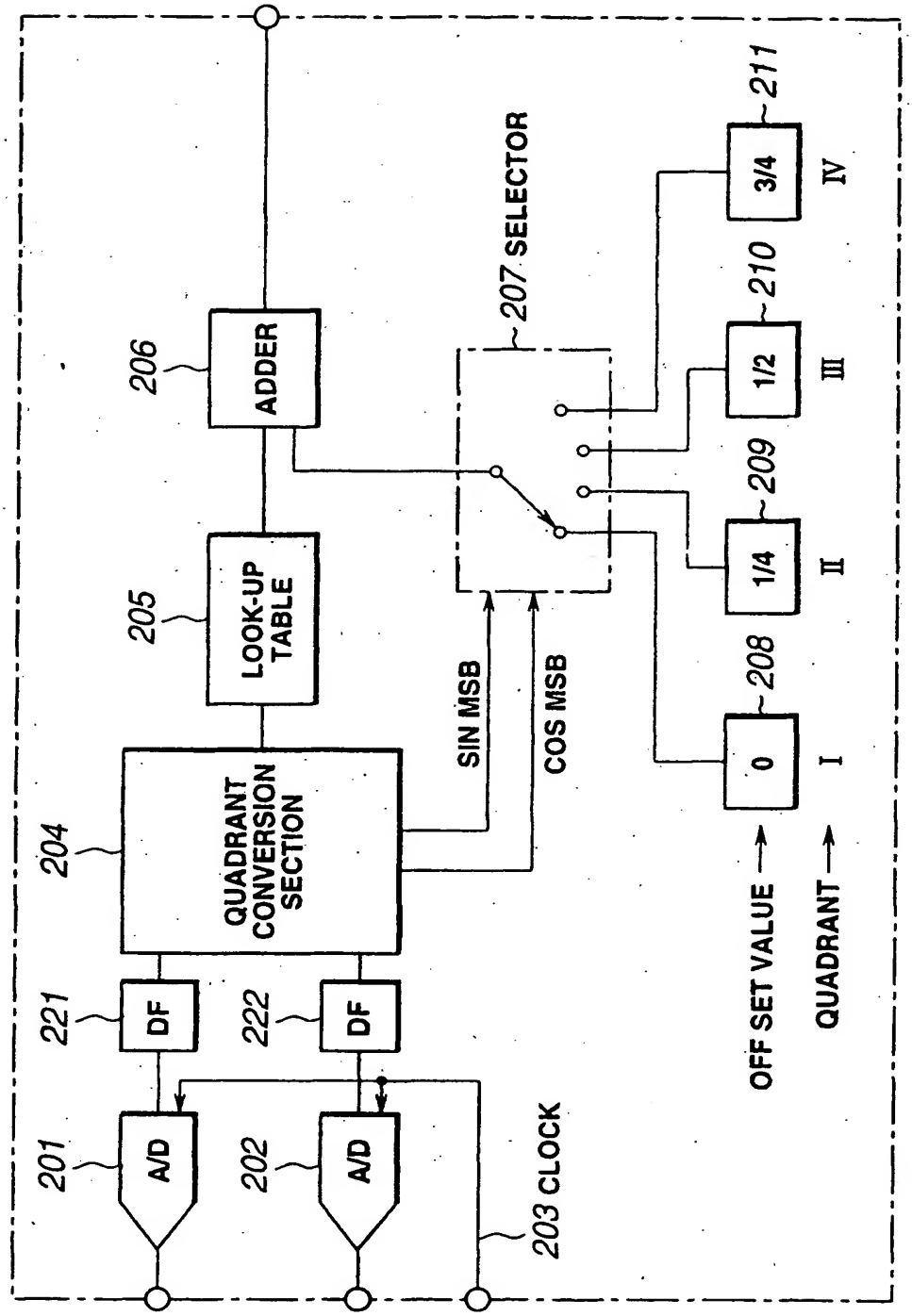

201
A/D
202
A/D
203 CLOCK
221
DF
222
DF
204
QUADRANT CONVERSION SECTION
205
LOOK-UP TABLE
206
ADDER
207 SELECTOR
SIN MSB
COS MSB
208
0
I
209
1/4
II
210
1/2
III
211
3/4
IV
OFF SET VALUE
QUADRANT

FIG.20

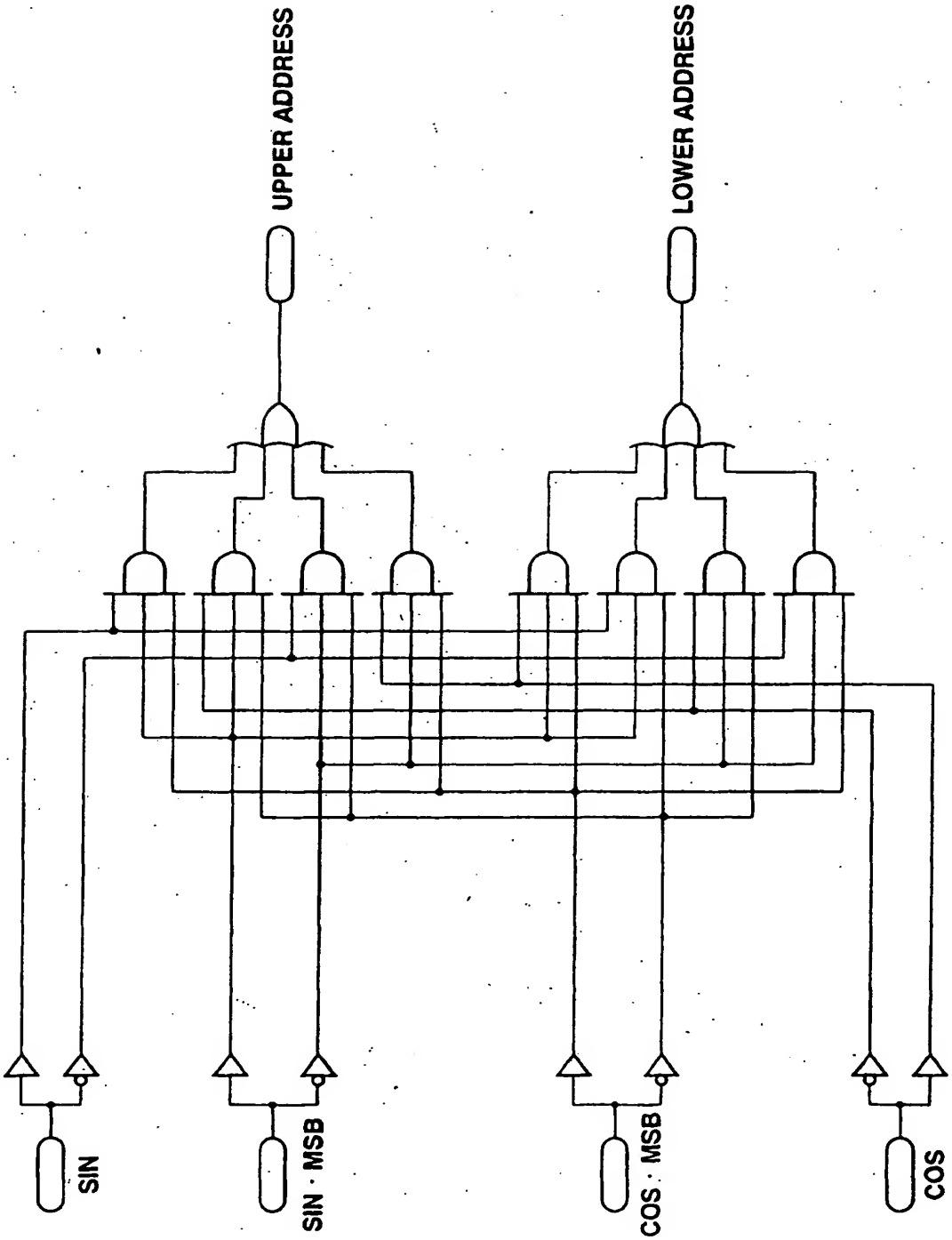


FIG.21

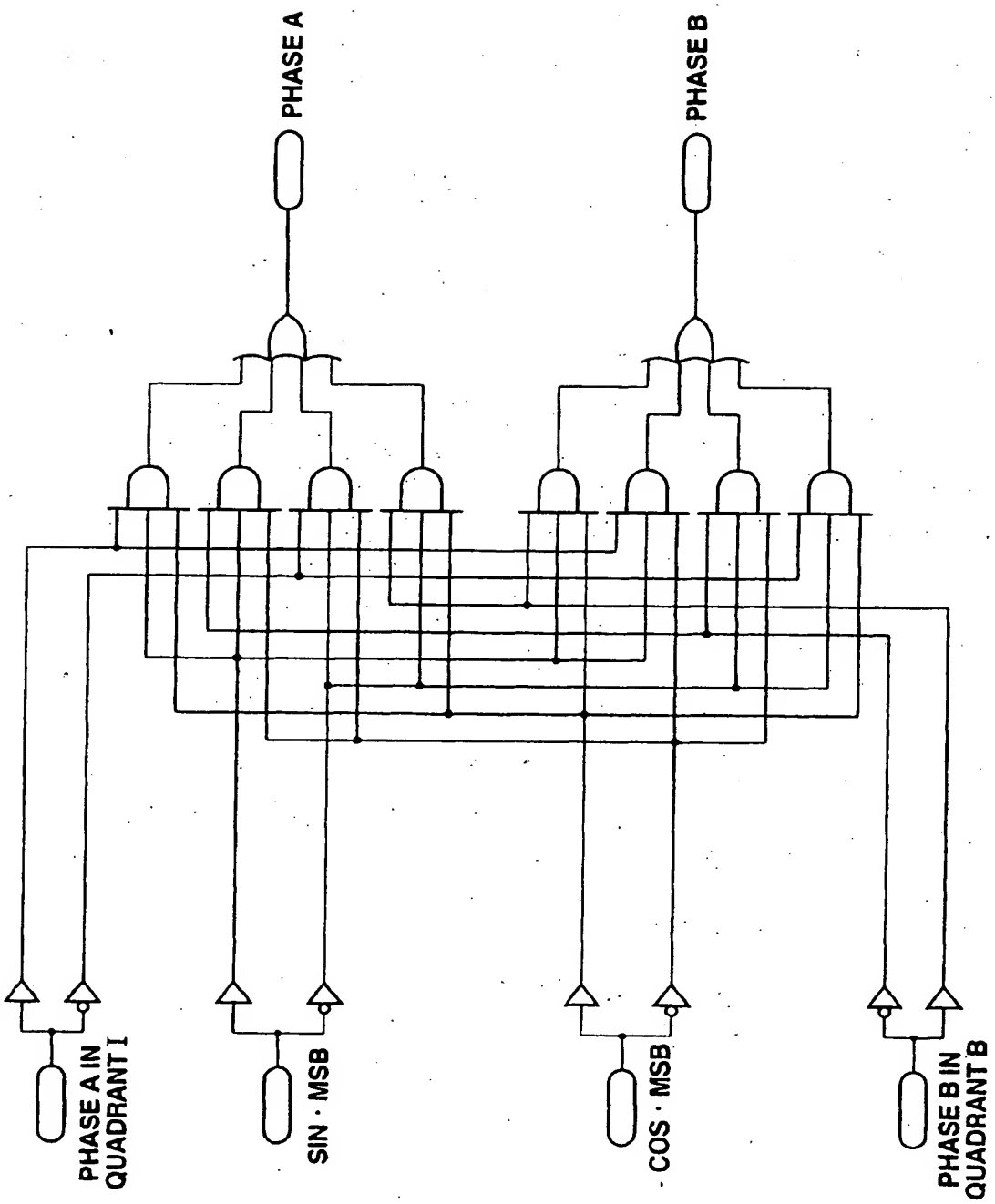

PHASE A
PHASE B
PHASE A IN QUADRANT I
SIN · MSB
COS · MSB
PHASE B IN QUADRANT B

FIG.22

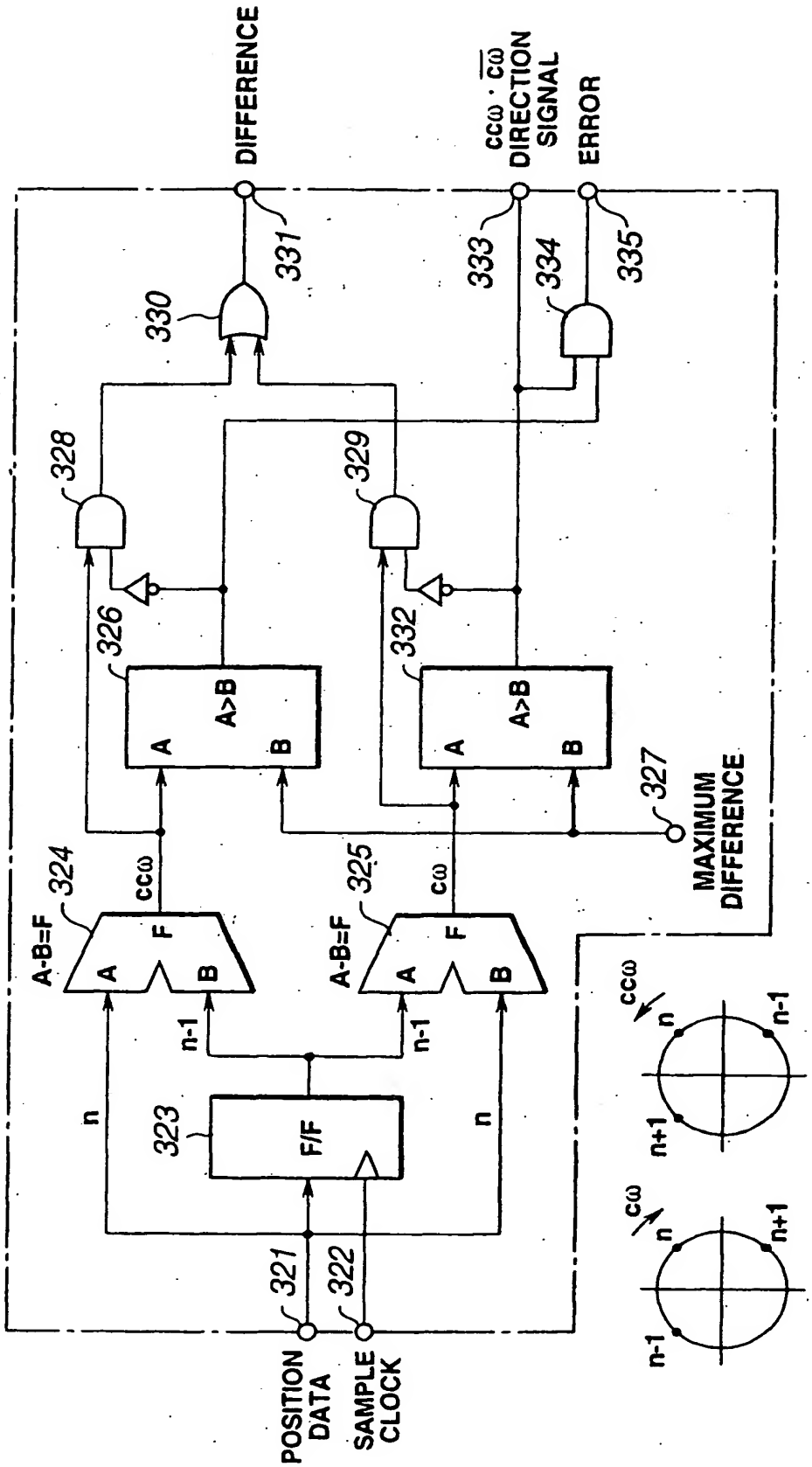
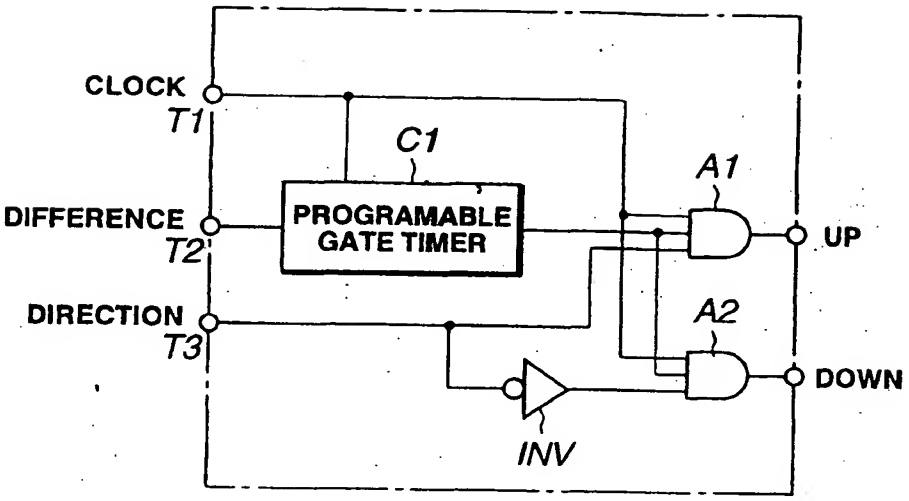
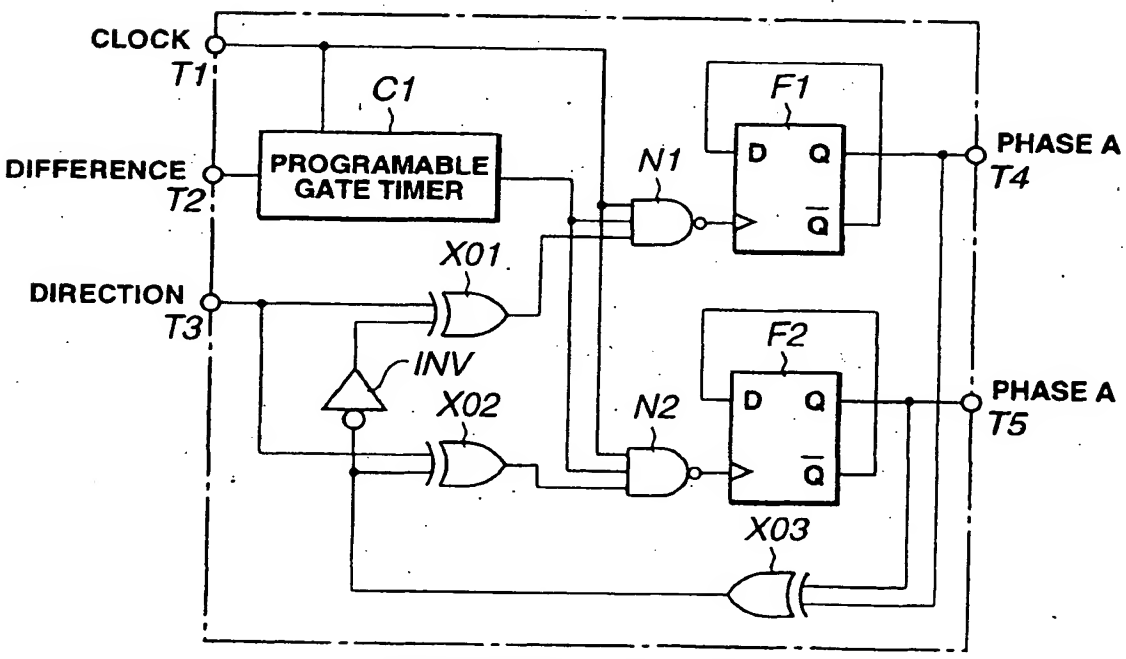

DIFFERENCE
ccω · c̄ω
DIRECTION SIGNAL
ERROR
331
333
334
335
330
328
329
326
332
A>B
A
B
327
MAXIMUM DIFFERENCE
324
325
A-B=F
F
ccω
cω
n
n-1
323
F/F
321
322
POSITION DATA
SAMPLE CLOCK
n+1

FIG.23



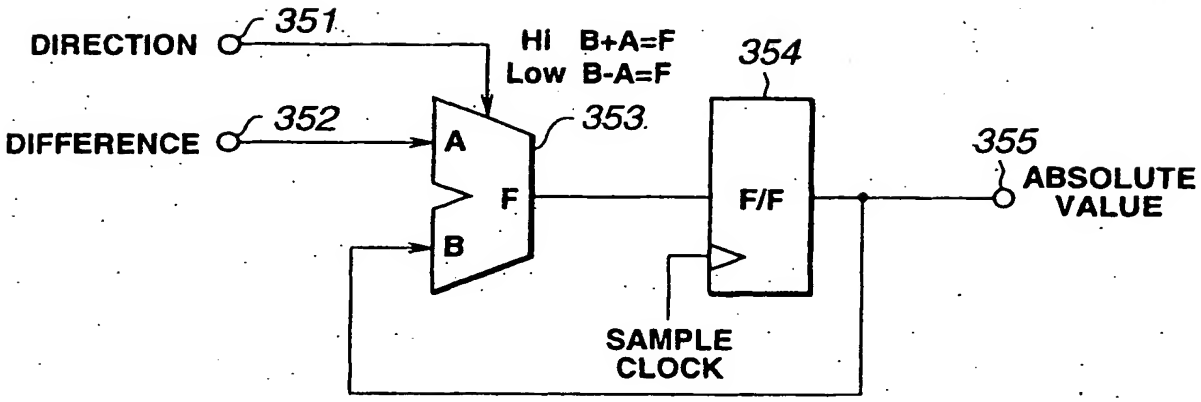
UP/DOWN CONVERSION

FIG.24



CONVERSION OF A/B PHASE

FIG.25


DIRECTION
351
Hi B+A=F
Low B-A=F
354
DIFFERENCE
352
353
A
F
B
F/F
355
ABSOLUTE VALUE
SAMPLE CLOCK